19-0870; Rev 1; 10/07

EEPROM-Based System Monitors with Nonvolatile Fault Memory

General Description

The MAX16031/MAX16032 EEPROM-configurable system monitors feature an integrated 10-bit analog-to-digital converter (ADC) designed to monitor voltages, temperatures, and current in complex systems. These EEPROM-configurable devices allow enormous flexibility in selecting operating ranges, upper and lower limits, fault output configuration, and operating modes with the capability of storing these values within the device.

The MAX16031 monitors up to eight voltages, three temperatures (one internal/two external remote temperature diodes), and a single current. The MAX16032 monitors up to six voltages and two temperatures (one internal/one remote temperature diode). Each of these monitored parameters is muxed into the ADC and written to its respective register that can be read back through the SMBus™ and JTAG interface.

Measured values are compared to the user-configurable upper and lower limits. For voltage measurements, there are two undervoltage and two overvoltage limits. For current and temperature, there are two sets of upper limits. Whenever the measured value is outside its limits, an alert signal is generated to notify the processor. Independent outputs are available for overcurrent, overtemperature, and undervoltage/overvoltage that are configured to assert on assigned channels. There are also undedicated fault outputs that are configured to offer a secondary limit for temperature, current, or voltage fault or provide a separate overvoltage output.

During a major fault event, such as a system shutdown, the MAX16031/MAX16032 automatically copy the internal ADC registers into the nonvolatile EEPROM registers that then are read back for diagnostic purposes.

The MAX16031/MAX16032 offer additional GPIOs that are used for voltage sequencing, additional fault outputs, a manual reset input, or read/write logic levels. A separate current-sense amplifier with an independent output allows for fast shutoff during overcurrent conditions. The MAX16031/MAX16032 are available in a 7mm x 7mm TQFN package and are fully specified from -40°C to +85°C.

Applications

Servers
Workstations
Storage Systems
Networking
Telecom

SMBus is a trademark of Intel Corp.

Features

- **Supply Voltage Operating Range of 2.85V to 14V**
- **Monitors Up to Eight Voltages (Single-Ended or Pseudo-Differential) with 1% Accuracy**
- **EEPROM-Configurable Limits**
  - **Two Undervoltage and Two Overvoltage**
  - **Two Overtemperature**
  - **Two Overcurrent**
- **High-Side Current-Sense Amplifier with Overcurrent Output (MAX16031 Only)**
- **Monitors Up to Three Temperatures (1 Internal/2 Remote)**
- **Nonvolatile Fault Memory Stores Fault Conditions for Later Retrieval**
- **Two Additional Configurable Fault Outputs**
- **Two Configurable GPIOs**
- **SMBus/I²C-Compatible Interface with $\overline{\text{ALERT}}$ Output and Bus Timeout Function**
- **JTAG Interface**
- **7mm x 7mm, 48-Pin TQFN Package**

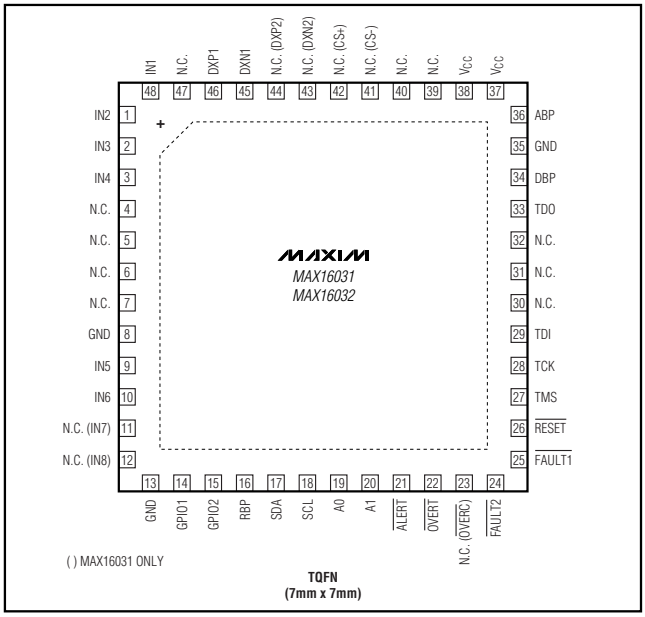
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX16031ETM+	-40°C to +85°C	48 TQFN-EP*	T4877-6
MAX16032ETM+	-40°C to +85°C	48 TQFN-EP*	T4877-6

+Denotes a lead-free package.

**EP = Exposed paddle.*

Pin Configuration

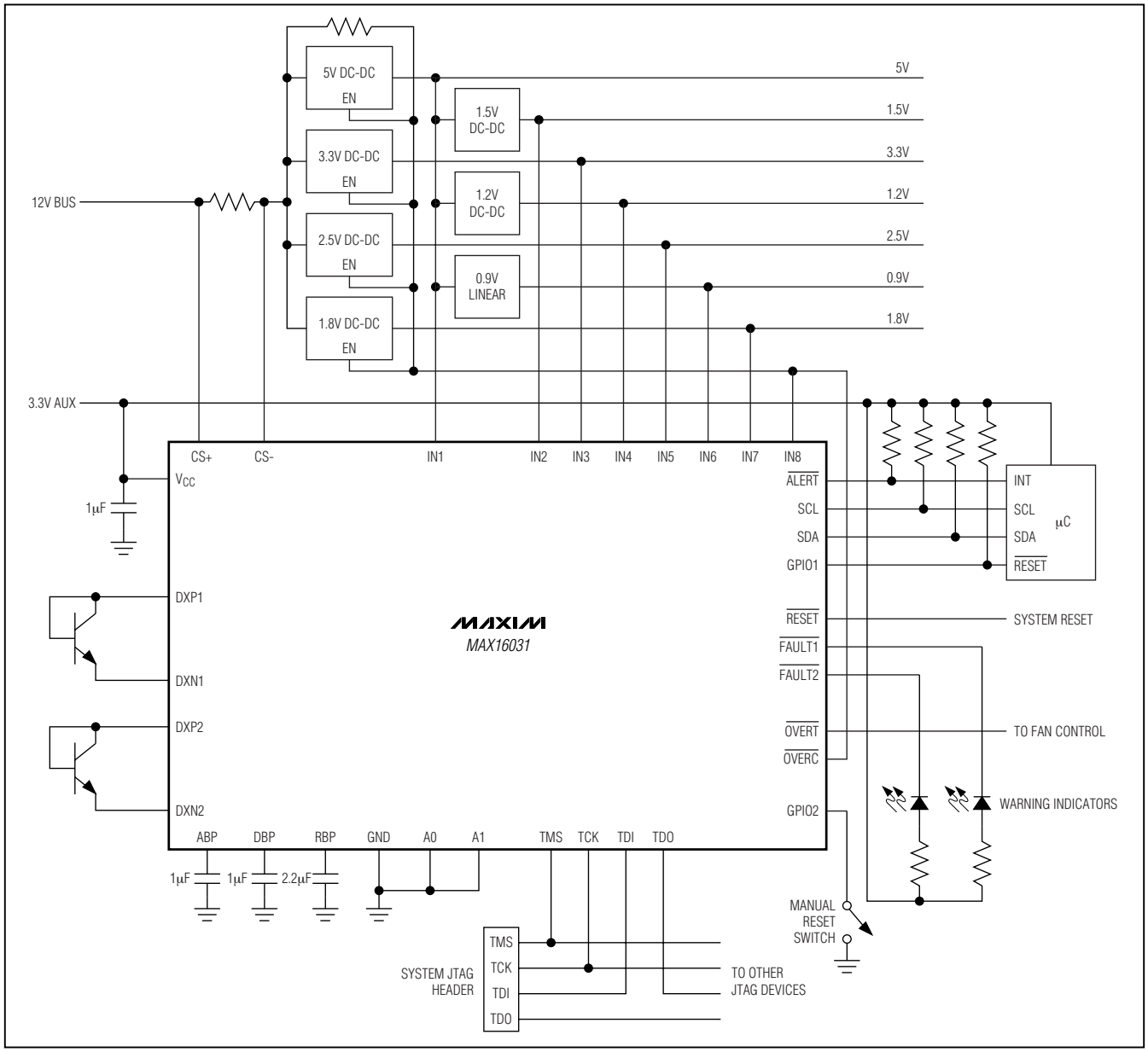


EEPROM-Based System Monitors with Nonvolatile Fault Memory

Selector Guide

PART	VOLTAGE MONITORS		TEMPERATURE SENSORS		CURRENT-SENSE AMPS	FAULT OUTPUTS	GPIOs
	SINGLE ENDED	DIFFERENTIAL	INT	EXT			
MAX16031ETM+	8	4	1	2	1	4	2
MAX16032ETM+	6	3	1	1	—	4	2

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +15V
IN_, FAULT_, SCL, SDA, $\overline{OVERT}$ to GND .....-0.3V to +6V
A0, A1, TCK, TMS, TDI to GND .....-0.3V to +6V
$\overline{OVERC}$, $\overline{RESET}$, GPIO_, $\overline{ALERT}$ to GND .....-0.3V to +6V
RBP, ABP, DBP to GND ...-0.3V to lower of (6V and V_{CC} + 0.3V)
TDO, DXP1, DXP2 to GND .....-0.3V to V_{DBP} + 0.3V
CS+, CS- to GND .....-0.3V to +30V
(CS+ - CS-) .....±5V
DXN1, DXN2 to GND .....-0.3V to +0.8V
SDA, $\overline{ALERT}$ Current .....-1mA to +50mA
DXN1, DXN2 Current 1mA
Input/Output Current
(all except DXN1, DXN2, SDA, and $\overline{ALERT}$) 20mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin, 7mm x 7mm TQFN
(derate 27.8mW/°C above +70°C) 2222.2mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.9V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		2.90		14.00	V
Undervoltage Lockout	V_{UVLO}	Minimum voltage at V_{CC} to access the digital interfaces			2.8	V
Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$			100		mV
Supply Current	I_{CC}	Static (EEPROM not accessed)		3	5	mA
ADC DC ACCURACY						
Resolution					10	Bits
Total Unadjusted Error		T_A = -40°C to +85°C			0.9	% FSR
Integral Nonlinearity				1		LSB
Differential Nonlinearity				1		LSB
ADC Total Monitoring Cycle Time	t_{CYCLE}	Eight supply inputs, three temperatures, and current sense		80	100	µs
ADC IN_ Voltage Ranges		Register map bit set to 00 (LSB = 5.46mV)		5.6		V
		Register map bit set to 01 (LSB = 2.73mV)		2.8		
		Register map bit set to 10 (LSB = 1.36mV)		1.4		
Reference Voltage	V_{RBP}		1.306	1.4	1.414	V
IN_ ANALOG INPUT						
Absolute Input Voltage Range (Referenced to GND)			0		5.6	V
Input Impedance			30	50	80	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.9V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Hysteresis		Percent of programmed threshold	r5Ch[5] = 0		0.78		%
			r5Ch[5] = 1		1.17		
RESET OUTPUT							
Reset Timeout Period	t_{RP}	r20h[5:3] = 000; from $\overline{MR}$ going high		22.5	25	27.5	µs
		r20h[5:3]= 001		2.25	2.5	2.75	ms
		r20h[5:3]= 010		9	10	11	
		r20h[5:3]= 011		36	40	44	
		r20h[5:3]= 100		144	160	176	
		r20h[5:3]= 101		576	640	704	
		r20h[5:3]= 110		1152	1280	1408	
		r20h[5:3]= 111		2304	2560	2816	
TEMPERATURE MEASUREMENTS							
Internal Sensor Measurement Error		(Note 2)			±3		°C
External Remote Diode Temperature Measurement Error		(Note 2)			±5		°C
Temperature Measurement Resolution					0.5		°C
Temperature Measurement Noise		Internal sensor			0.1		°C
External Diode Drive High					84		µA
External Diode Drive Low					6		µA
Diode Drive Current Ratio					14		
DXN_ Impedance to GND					1.8		kΩ
Power-Supply Rejection	PSR	Internal sensor, DC condition			0.1		°C/V
CURRENT SENSE							
CS+ Input Voltage Range	V_{CS+}			3		28	V
Input Bias Current	I_{CS+}	V_{CS+} = V_{CS-}			14	25	µA
	I_{CS-}	V_{CS-} = V_{CS+}			3	8	
Primary Current-Sense Differential Thresholds	V_{CSTH}	V_{CS+} - V_{CS-}	A = 48	21.5	25	28.5	mV
			A = 24	45	50	55	
			A = 12	92	100	108	
			A = 6	190	200	210	
Primary Current-Sense Threshold	CS_{HYS}	Percent of V_{CSTH}			0.5		%
Secondary Overcurrent Threshold Timeout		r5Ch[1:0] = 00			50		µs
		r5Ch[1:0] = 01		3.6	4	4.4	ms
		r5Ch[1:0] = 10		14.4	16	17.6	
		r5Ch[1:0] = 11		57.6	64	70.4	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.9V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Sense Analog Input Range		V_{CS+} - V_{CS-}	A = 6		232		mV
			A = 12		116		
			A = 24		58		
			A = 48		29		
ADC Current-Sense Measurement Accuracy		V_{SENSE} = 150mV, (A = 6 only)		-4	±0.2	+4	%
		V_{SENSE} = 50mV, (A = 6, 12 only)		-10	±1.2	+10	
		V_{SENSE} = 25mV			±2		
		V_{SENSE} = 10mV			±10		
Gain Accuracy		V_{SENSE} = 20mV to 100mV, V_{CS+} = 12V, A = 6		-3		+3	%
Common-Mode Rejection Ratio	$CMRR_{CS}$	V_{CS+} > 4V			80		dB
Power-Supply Rejection Ratio	$PSRR_{CS}$				80		dB
$\overline{OVERC}$ Output Leakage Current	$I_{OVERCLKG}$					1	µA
$\overline{OVERC}$ Output Low Voltage	$V_{OLOVERC}$	I_{OUT} = 3mA				0.4	V
$\overline{OVERC}$ Propagation Delay	t_{OVERC}	V_{SENSE} - V_{CSTH} > 10% x V_{CSTH}				5	µs
SMBus INTERFACE (SCL, SDA)							
Logic-Input Low Voltage	V_{IL}	Input voltage falling				0.8	V
Logic-Input High Voltage	V_{IH}	Input voltage rising		2.0			V
Input Leakage Current		GND or 5.5V (V_{CC} = 5.5V) V_{SCL}, V_{SDA}		-1		+1	µA
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
Input Capacitance	C_{IN}				5		pF
$\overline{ALERT}$, $\overline{FAULT\_}$, AND GPIO_ OUTPUTS							
$\overline{ALERT}$, $\overline{FAULT\_}$, and GPIO_ Output Low Voltage		I_{SINK} = 3mA				0.4	V
$\overline{ALERT}$, $\overline{FAULT\_}$, and GPIO_ Leakage Current		$V_{\overline{ALERT}}$, $V_{\overline{FAULT}}$, $V_{GPIO\_}$ = 5.5V or GND		-1		+1	µA
GPIO_ (INPUT)							
Logic-Low Voltage		GPIO_ voltage falling				0.8	V
Logic-High Voltage		GPIO_ voltage rising		2.0			V
SMBus ADDRESS (A0 and A1)							
Address Logic-Low						0.4	V
Address Logic-High				1.4			V
High-Impedance Leakage Current		Maximum current to achieve high-impedance logic level		-1		+1	µA
Input Leakage Current		0 to 3V, V_{CC} = 3V		-12		+12	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.9V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus TIMING (see Figure 1)						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Output Fall Time	t_{OF}	C_{BUS} = 10pF to 400pF			250	ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0.3		0.9	µs
Minimum Pulse Width Ignored				30		ns
SMBus Timeout	$t_{TIMEOUT}$	SCL time low for reset	25		35	ms
JTAG INTERFACE (see Figure 2)						
TDI, TMS, TCK Logic-Low Input Voltage	V_{IL}	Input voltage falling			0.4	V
TDI, TMS, TCK Logic-High Input Voltage	V_{IH}	Input voltage rising	2.2			V
TDO Logic-Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.4	V
TDO Logic-Output High Voltage	V_{OH}	I_{SOURCE} = 1mA	2.2			V
TDO Leakage Current		TDO high impedance	-10		+10	µA
TDI, TMS Pullup Resistors	R_{JPU}	Pullup to V_{DBP}	6.5	10	16	kΩ
I/O Capacitance	$C_{I/O}$			50		pF
TCK Clock Period	t_1				1000	ns
TCK High/Low Time	t_2, t_3	(Note 3)	60	500		ns
TCK to TMS, TDI Setup Time	t_4		15			ns
TCK to TMS, TDI Hold Time	t_5		35			ns
TCK to TDO Delay	t_6				500	ns
TCK to TDO High-Impedance Delay	t_7				500	ns
MISCELLANEOUS						
Power-On Delay	t_{D-PO}				4	ms
Single-Byte EEPROM Write Cycle Delay		(Note 4)			11	ms

Note 1: Limits to -40°C are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: TCK stops either high or low.
Note 4: An additional cycle is required when writing to configuration memory for the first time.

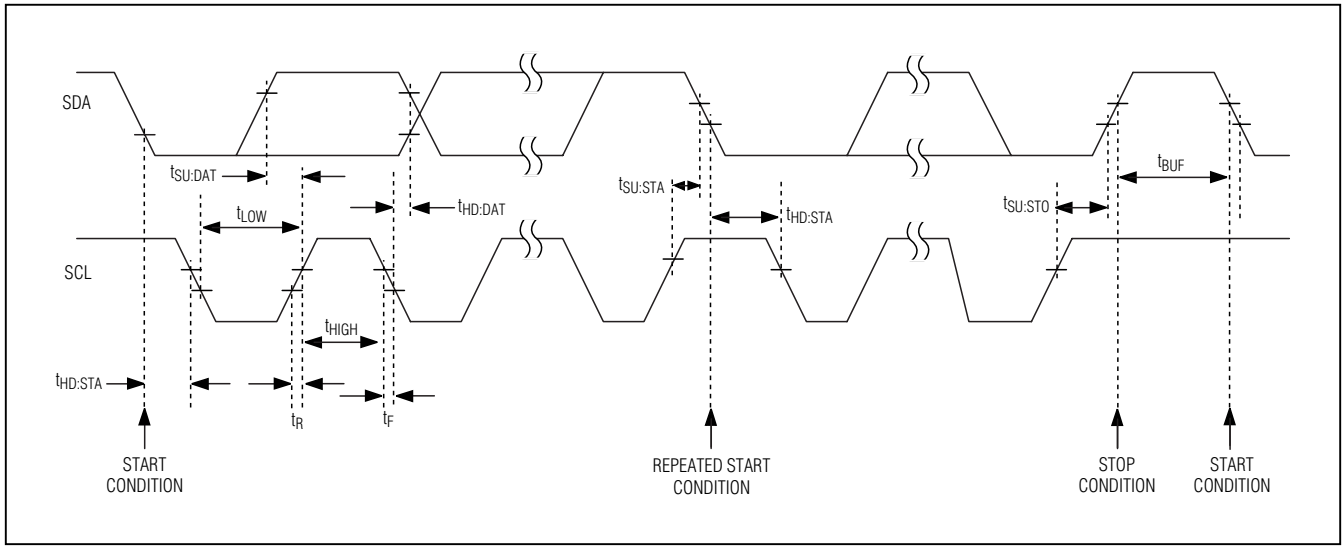


Figure 1. SMBus Interface Timing Diagram

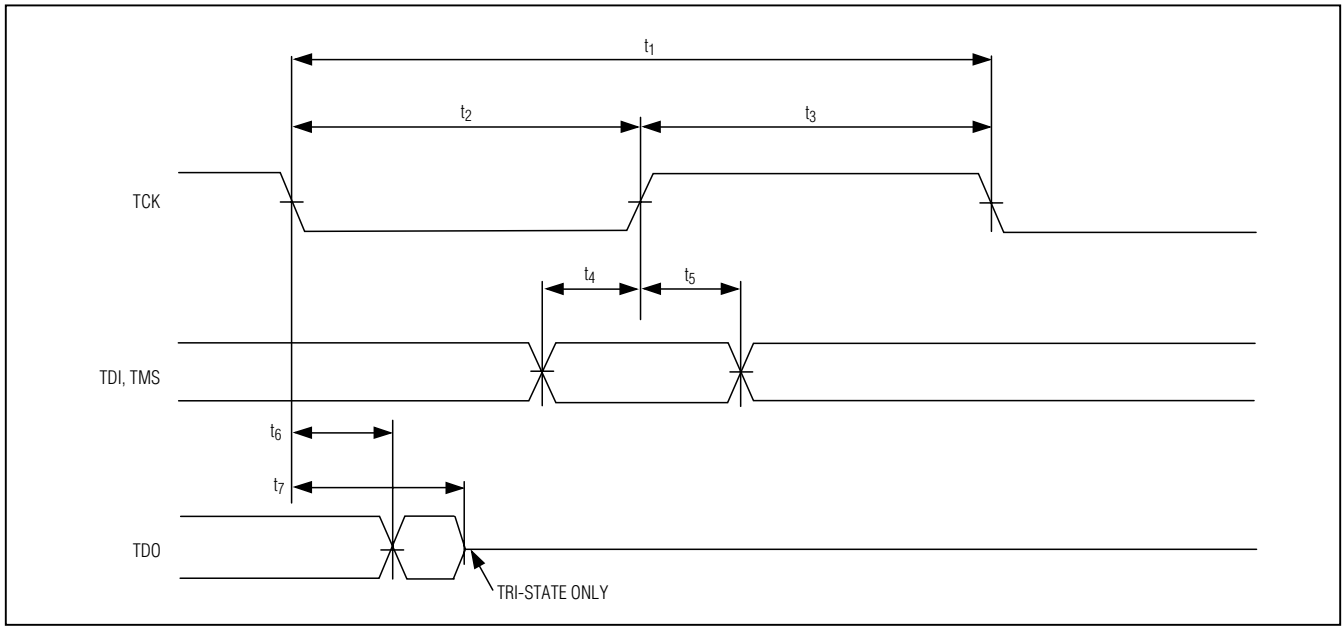


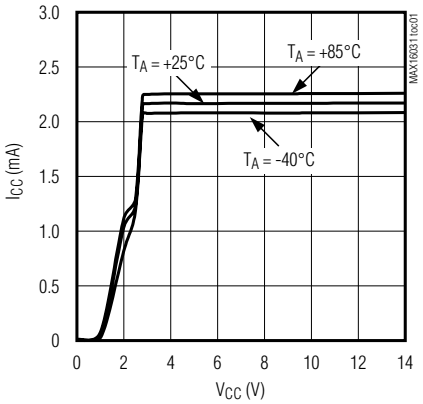
Figure 2. JTAG Interface Timing Diagram

EEPROM-Based System Monitors with Nonvolatile Fault Memory

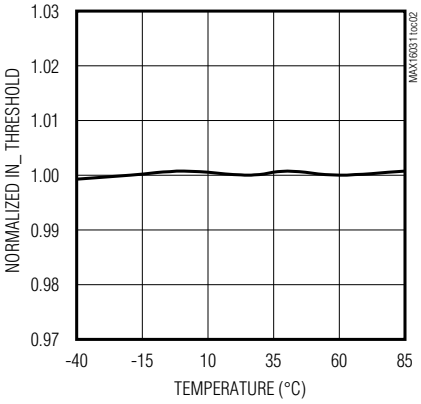
Typical Operating Characteristics

(Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

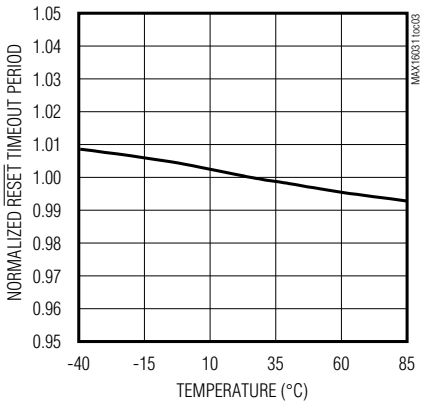
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



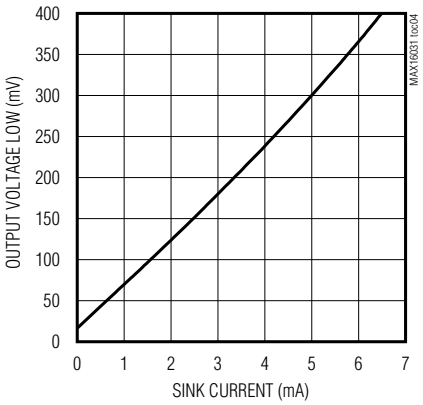
NORMALIZED IN_ THRESHOLD vs. TEMPERATURE



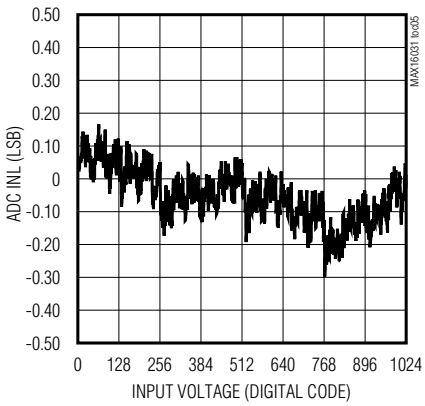
NORMALIZED $\overline{RESET}$ TIMEOUT PERIOD vs. TEMPERATURE



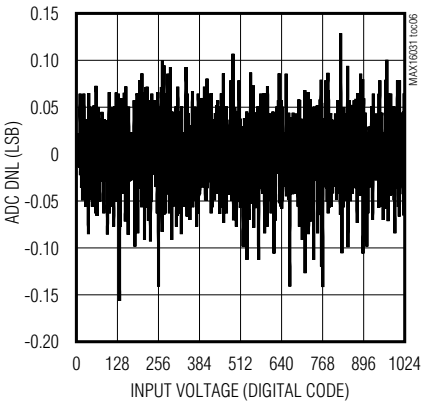
OUTPUT VOLTAGE LOW vs. SINK CURRENT



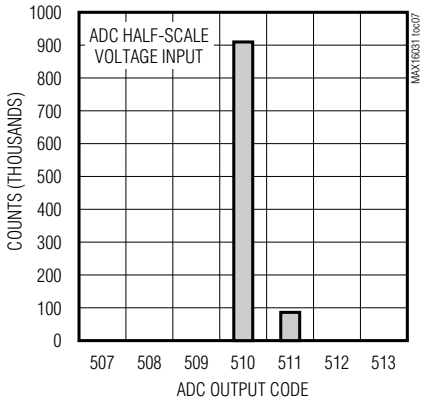
ADC INTEGRAL NONLINEARITY vs. INPUT VOLTAGE



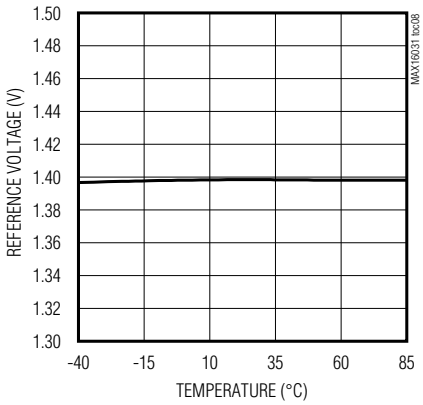
ADC DIFFERENTIAL NONLINEARITY vs. INPUT VOLTAGE



NOISE HISTOGRAM



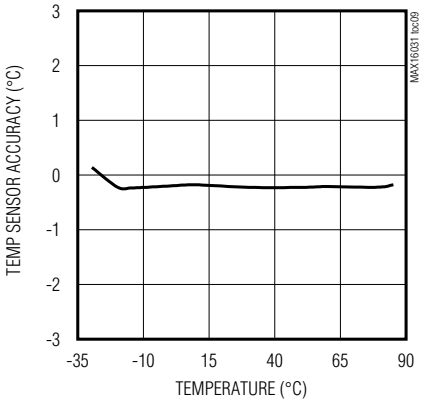
REFERENCE VOLTAGE vs. TEMPERATURE



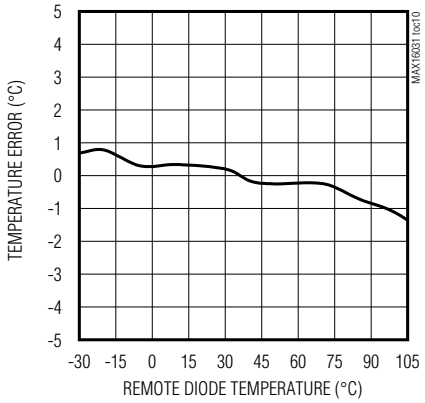
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

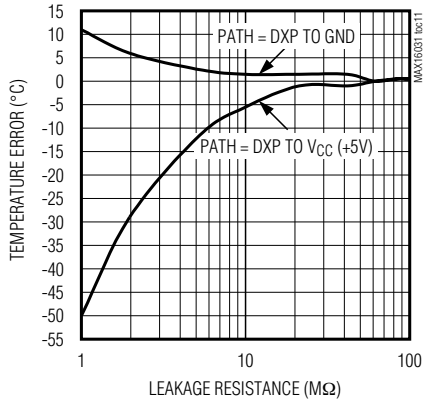
INTERNAL TEMPERATURE SENSOR ACCURACY vs. TEMPERATURE



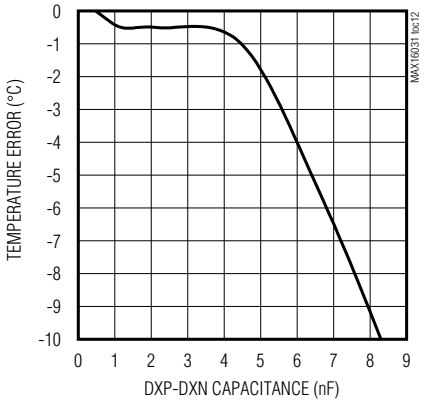
TEMPERATURE ERROR vs. REMOTE DIODE TEMPERATURE



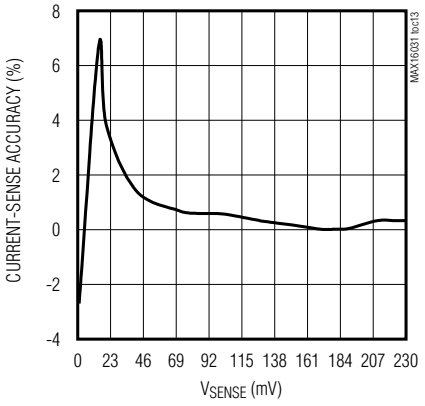
TEMPERATURE ERROR vs. LEAKAGE RESISTANCE



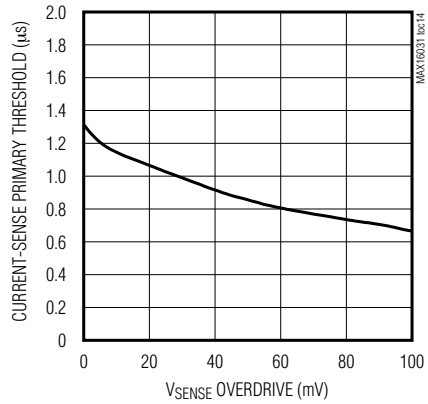
TEMPERATURE ERROR vs. DXP-DXN CAPACITANCE



CURRENT-SENSE ACCURACY vs. V_{SENSE}



CURRENT-SENSE PRIMARY THRESHOLD vs. V_{SENSE} OVERDRIVE



EEPROM-Based System Monitors with Nonvolatile Fault Memory

Pin Description

PIN		NAME	FUNCTION
MAX16031	MAX16032		
1	1	IN2	Supply Monitor Input 2. IN2 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN1 and IN2 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
2	2	IN3	Supply Monitor Input 3. IN3 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN3 and IN4 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
3	3	IN4	Supply Monitor Input 4. IN4 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN3 and IN4 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
4–7, 30, 31, 32, 39, 40, 47	4–7, 11, 12, 23, 30, 31, 32, 39, 40–44, 47	N.C.	No Connection. Leave unconnected. Do not use.
8, 13, 35	8, 13, 35	GND	Ground. Connect all GND pins together.
9	9	IN5	Supply Monitor Input 5. IN5 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN5 and IN6 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
10	10	IN6	Supply Monitor Input 6. IN6 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN5 and IN6 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
11	—	IN7	Supply Monitor Input 7. IN7 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN7 and IN8 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
12	—	IN8	Supply Monitor Input 8. IN8 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN7 and IN8 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
14	14	GPIO1	Configurable General-Purpose Input/Output 1
15	15	GPIO2	Configurable General-Purpose Input/Output 2
16	16	RBP	ADC Reference Bypass. RBP is an internally generated 1.4V reference for the ADC. Bypass RBP to GND with a 2.2µF capacitor. Do not use RBP to power any additional circuitry.
17	17	SDA	SMBus Serial-Data, Open-Drain Input/Output
18	18	SCL	SMBus Serial-Clock Input
19	19	A0	SMBus Address Input 0. Connect to DBP, GND, or leave unconnected to select the desired device address.
20	20	A1	SMBus Address Input 1. Connect to DBP, GND, or leave unconnected to select the desired device address.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX16031	MAX16032		
21	21	$\overline{ALERT}$	SMBus Alert Open-Drain Output. $\overline{ALERT}$ follows the SMBALERT# signal functionality described in Appendix A of the SMBus 2.0 Specification. $\overline{ALERT}$ asserts when the device detects a fault, thereby interrupting the host processor to query which device on the serial bus detected faults.
22	22	$\overline{OVERT}$	Overtemperature, Open-Drain Output. $\overline{OVERT}$ asserts when an overtemperature condition is detected.
23	—	$\overline{OVERC}$	Overcurrent, Open-Drain Output. $\overline{OVERC}$ asserts when the primary overcurrent threshold is exceeded.
24	24	$\overline{FAULT2}$	Configurable Open-Drain Fault Output 2
25	25	$\overline{FAULT1}$	Configurable Open-Drain Fault Output 1
26	26	$\overline{RESET}$	Configurable Open-Drain Reset Output
27	27	TMS	JTAG Test Mode Select Input. Internally pulled up to V_{DBP} with a 10kΩ resistor.
28	28	TCK	JTAG Test Clock Input
29	29	TDI	JTAG Test Data Input. Internally pulled up to V_{DBP} with a 10kΩ resistor.
33	33	TDO	JTAG Test Data Output
34	34	DBP	Internal Digital Voltage Regulator Output. Connect a 1µF bypass capacitor from DBP to GND. Do not use DBP to power external circuitry.
36	36	ABP	Internal Analog Voltage Regulator Output. Connect a 1µF bypass capacitor from ABP to GND. Do not use ABP to power external circuitry.
37, 38	37, 38	V_{CC}	Device Power Supply. Bypass V_{CC} to GND with a 1µF capacitor.
41	41	CS-	Current-Sense Negative Input. Must be biased between 3V to 28V for proper operation.
42	42	CS+	Current-Sense Positive Input. Must be biased between 3V to 28V for proper operation.
43	—	DXN2	Remote Diode 2 Negative Input. If remote sensing is not used, connect DXP2 to DXN2.
44	—	DXP2	Remote Diode 2 Positive Input. If remote sensing is not used, connect DXP2 to DXN2.
45	45	DXN1	Remote Diode 1 Negative Input. If remote sensing is not used, connect DXP1 to DXN1.
46	46	DXP1	Remote Diode 1 Positive Input. If remote sensing is not used, connect DXP1 to DXN1.
48	48	IN1	Supply Monitor Input 1. IN1 is internally sampled by the ADC. It is configurable for unipolar/bipolar and single-ended/pseudo-differential. In pseudo-differential mode, IN1 and IN2 form the + and - of the differential pair. Each input must stay within the specified ADC IN_ voltage range.
—	—	EP	Exposed Paddle. Connect EP to ground. EP is internally connected to GND. Do not use as the main ground connection.

EEPROM-Based System Monitors with Nonvolatile Fault Memory

Functional Diagram

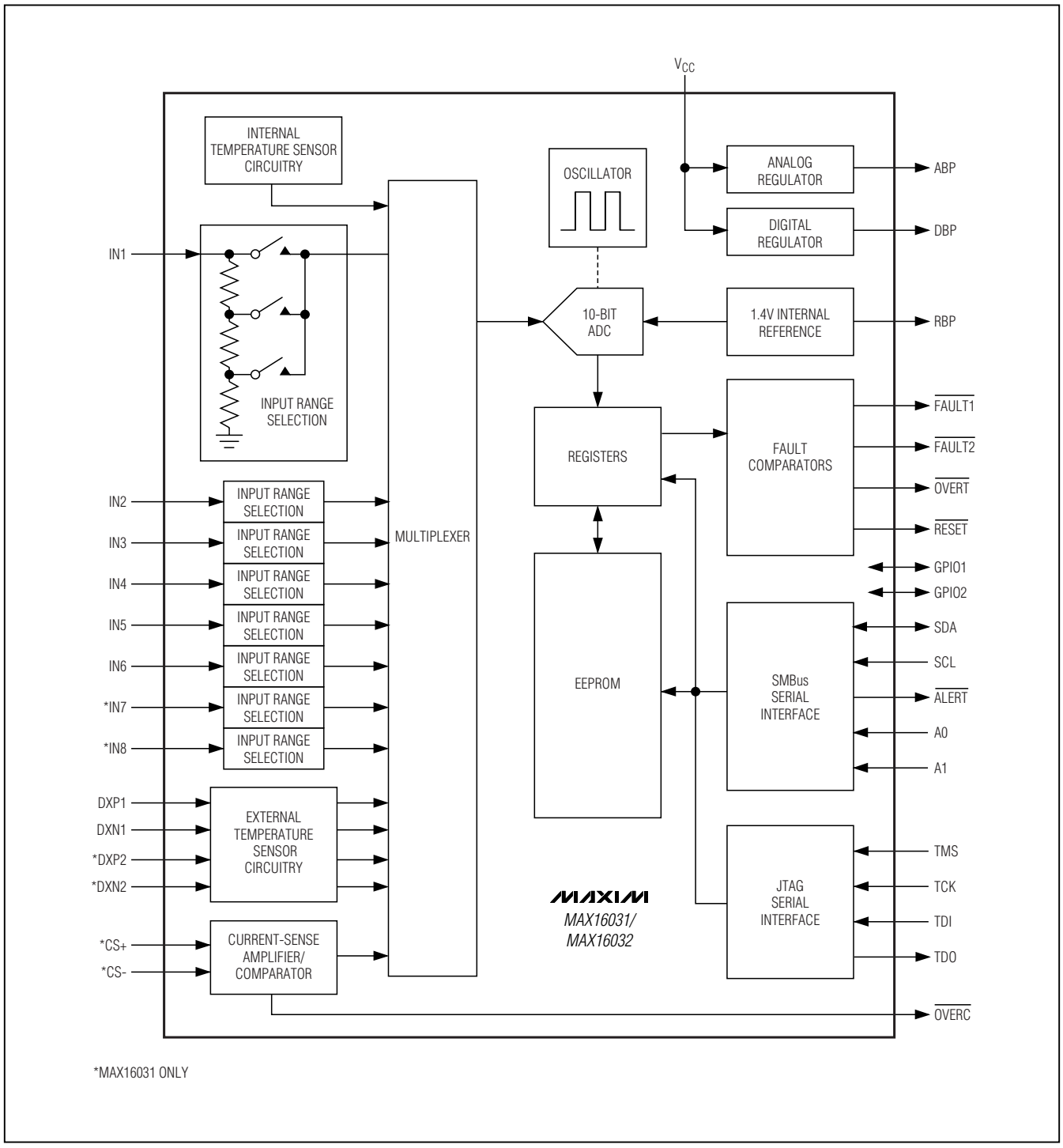


Table 1. Address Map

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
00h	—	R	IN1 ADC Result Register (MSB)
01h	—	R	IN1 ADC Result Register (LSB)
02h	—	R	IN2 ADC Result Register (MSB)
03h	—	R	IN2 ADC Result Register (LSB)
04h	—	R	IN3 ADC Result Register (MSB)
05h	—	R	IN3 ADC Result Register (LSB)
06h	—	R	IN4 ADC Result Register (MSB)
07h	—	R	IN4 ADC Result Register (LSB)
08h	—	R	IN5 ADC Result Register (MSB)
09h	—	R	IN5 ADC Result Register (LSB)
0Ah	—	R	IN6 ADC Result Register (MSB)
0Bh	—	R	IN6 ADC Result Register (LSB)
0Ch	—	R	IN7 ADC Result Register (MSB)*
0Dh	—	R	IN7 ADC Result Register (LSB)*
0Eh	—	R	IN8 ADC Result Register (MSB)*
0Fh	—	R	IN8 ADC Result Register (LSB)*
10h	—	R	Internal Temperature Sensor ADC Result Register (MSB)
11h	—	R	Internal Temperature Sensor ADC Result Register (LSB)
12h	—	R	Remote Temperature Sensor 1 ADC Result Register (MSB)
13h	—	R	Remote Temperature Sensor 1 ADC Result Register (LSB)
14h	—	R	Remote Temperature Sensor 2 ADC Result Register (MSB)
15h	—	R	Remote Temperature Sensor 2 ADC Result Register (LSB)
16h	—	R	Current-Sense ADC Result Register
17h	97h	R/W	Voltage Monitoring Input ADC Range Selection (IN1–IN4)
18h	98h	R/W	Voltage Monitoring Input ADC Range Selection (IN5–IN8)
19h	99h	R/W	Current-Sense Gain/Primary Threshold and Remote Temperature Sensor 1 Gain Trim
1Ah	9Ah	R/W	Voltage Monitoring Input Enable
1Bh	9Bh	R/W	Internal/Remote Temperature Sensor, Current Sense, and $\overline{\text{ALERT}}$ Enables and Remote Temperature Sensor 1 Offset Trim
1Ch	9Ch	R/W	Voltage Monitoring Input Single-Ended/Differential and Unipolar/Bipolar Selection
1Dh	9Dh	R/W	$\overline{\text{FAULT1}}$ Dependency Selection
1Eh	9Eh	R/W	$\overline{\text{FAULT2}}$ Dependency Selection
1Fh	9Fh	R/W	$\overline{\text{OVERT}}$ Dependency Selection
20h	A0h	R/W	$\overline{\text{RESET}}$ Dependency and Timeout Selection
21h	A1h	R/W	$\overline{\text{RESET}}$ IN1–IN8 Dependency Selection
22h	A2h	R/W	GPIO1 Configuration
23h	A3h	R/W	GPIO1 Dependency Selection
24h	A4h	R/W	GPIO2 Configuration

Table 1. Address Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
25h	A5h	R/W	GPIO2 Dependency Selection
26h	A6h	R/W	IN1 Primary Undervoltage Threshold
27h	A7h	R/W	IN1 Primary Overvoltage Threshold
28h	A8h	R/W	IN1 Secondary Undervoltage Threshold
29h	A9h	R/W	IN1 Secondary Overvoltage Threshold
2Ah	AAh	R/W	IN2 Primary Undervoltage Threshold
2Bh	ABh	R/W	IN2 Primary Overvoltage Threshold
2Ch	ACh	R/W	IN2 Secondary Undervoltage Threshold
2Dh	ADh	R/W	IN2 Secondary Overvoltage Threshold
2Eh	AEh	R/W	IN3 Primary Undervoltage Threshold
2Fh	AFh	R/W	IN3 Primary Overvoltage Threshold
30h	B0h	R/W	IN3 Secondary Undervoltage Threshold
31h	B1h	R/W	IN3 Secondary Overvoltage Threshold
32h	B2h	R/W	IN4 Primary Undervoltage Threshold
33h	B3h	R/W	IN4 Primary Overvoltage Threshold
34h	B4h	R/W	IN4 Secondary Undervoltage Threshold
35h	B5h	R/W	IN4 Secondary Overvoltage Threshold
36h	B6h	R/W	IN5 Primary Undervoltage Threshold
37h	B7h	R/W	IN5 Primary Overvoltage Threshold
38h	B8h	R/W	IN5 Secondary Undervoltage Threshold
39h	B9h	R/W	IN5 Secondary Overvoltage Threshold
3Ah	BAh	R/W	IN6 Primary Undervoltage Threshold
3Bh	BBh	R/W	IN6 Primary Overvoltage Threshold
3Ch	BCh	R/W	IN6 Secondary Undervoltage Threshold
3Dh	BDh	R/W	IN6 Secondary Overvoltage Threshold
3Eh	BEh	R/W	IN7 Primary Undervoltage Threshold*
3Fh	BFh	R/W	IN7 Primary Overvoltage Threshold*
40h	C0h	R/W	IN7 Secondary Undervoltage Threshold*
41h	C1h	R/W	IN7 Secondary Overvoltage Threshold*
42h	C2h	R/W	IN8 Primary Undervoltage Threshold*
43h	C3h	R/W	IN8 Primary Overvoltage Threshold*
44h	C4h	R/W	IN8 Secondary Undervoltage Threshold*
45h	C5h	R/W	IN8 Secondary Overvoltage Threshold*
46h	C6h	R/W	Internal Temperature Sensor Primary Overtemperature Threshold (MSB)
47h	C7h	R/W	Internal Temperature Sensor Secondary Overtemperature Threshold (MSB)
48h	C8h	R/W	Remote Temperature Sensor 1 Primary Overtemperature Threshold
49h	C9h	R/W	Remote Temperature Sensor 1 Secondary Overtemperature Threshold
4Ah	CAh	R/W	Remote Temperature Sensor 2 Primary Overtemperature Threshold

Table 1. Address Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
4Bh	CBh	R/W	Remote Temperature Sensor 2 Secondary Overtemperature Threshold
4Ch	CCh	R/W	Overcurrent Secondary Threshold
4Dh	CDh	R/W	Remote Temperature Sensor Primary/Secondary Overtemperature Threshold (LSBs). External Temperature Sensor 2 Offset Trim
4Eh	CEh	R/W	Remote Temperature Sensor 1/2 Primary/Secondary Overtemperature Threshold (LSBs)
4Fh	CFh	R/W	Remote Temperature Sensor 2 Gain Trim
50h	D0h	R/W	Remote Temperature Sensor Short/Open Status
51h	D1h	R/W	IN1–IN8 Primary Threshold Fault Status
52h	D2h	R/W	IN1–IN8 Secondary Threshold Fault Status
53h	D3h	R/W	Temperature/Current Threshold Fault Status
54h	D4h	R/W	Remote Temperature Sensor Short/Open Fault Mask
55h	D5h	R/W	IN1–IN8 Primary Threshold Fault Mask
56h	D6h	R/W	IN1–IN8 Secondary Threshold Fault Mask
57h	D7h	R/W	Temperature/Current Threshold Fault Mask
58h	D8h	R/W	IN1–IN8 Primary Undervoltage Faults Triggering Fault EEPROM
59h	D9h	R/W	IN1–IN8 Primary Overvoltage Faults Triggering Fault EEPROM
5Ah	DAh	R/W	Temperature/Current Faults Triggering Fault EEPROM
5Bh	DBh	R/W	Temperature Filter Selection and Postboot Fault Mask Time
5Ch	DCh	R/W	Threshold Fault Options and Overcurrent Fault Timeout
5Dh	DDh	—	Reserved
5Eh	DEh	R/W	Customer Firmware Version
5Fh	DFh	R/W	EEPROM and Configuration Lock
60h–7Fh	E0h–FFh	—	Reserved
—	80h	R	IN1–IN8 Primary Threshold Fault Status at Time of Fault
—	81h	R	IN1–IN8 Secondary Threshold Fault Status at Time of Fault
—	82h	R	Temperature/Current Threshold Fault Status at Time of Fault
—	83h	R	IN1 Conversion Result at Time of Fault
—	84h	R	IN2 Conversion Result at Time of Fault
—	85h	R	IN3 Conversion Result at Time of Fault
—	86h	R	IN4 Conversion Result at Time of Fault
—	87h	R	IN5 Conversion Result at Time of Fault
—	88h	R	IN6 Conversion Result at Time of Fault
—	89h	R	IN7 Conversion Result at Time of Fault*
—	8Ah	R	IN8 Conversion Result at Time of Fault*
—	8Bh	R	Internal Temperature Sensor Conversion Result at Time of Fault
—	8Ch	R	Remote Temperature Sensor 1 Conversion Result at Time of Fault
—	8Dh	R	Remote Temperature Sensor 2 Conversion Result at Time of Fault*
—	8Eh	R	Current-Sense Conversion Result at Time of Fault*

**MAX16031 only.*

EEPROM-Based System Monitors with Nonvolatile Fault Memory

Detailed Description

Getting Started

The MAX16031/MAX16032 contain both I²C/SMBus and JTAG serial interfaces for accessing registers and EEPROM. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *I²C/SMBus-Compatible Serial Interface* and *JTAG Serial Interface* sections. This data sheet uses a specific convention for referring to bits within a particular address location. As an example, r15h[3:0] refers to bits 3 through 0 in register with address 15 hexadecimal.

The factory-default values at power-on reset (POR) for all EEPROM locations are zeros. POR occurs when V_{CC} reaches the undervoltage lockout (UVLO) of 2.8V. At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and EEPROM contents are copied to the respective register locations. The boot-up sequence takes up to 1.81ms. Monitoring is disabled for up to 16s past the boot-up sequence by programming r5Bh[3:0] (see the *Miscellaneous Settings* section). $\overline{\text{RESET}}$ is low during boot-up and remains low after boot-up for its programmed timeout period after all monitored channels are within their respective thresholds.

The MAX16031/MAX16032 monitor up to eight voltages, up to one current, and up to three temperatures. After boot-up, an internal multiplexer cycles through each input. At each multiplexer stop, the 10-bit ADC converts the analog parameter to a digital result and stores the result in a register. Each time the multiplexer completes a cycle, internal logic compares the conversion results to the thresholds stored in memory. When a conversion violates a programmed threshold, the conversion is configured to generate a fault. Logic outputs are programmed to depend on many combinations of faults. Additionally, faults are programmed to trigger a fault log, whereby all fault information is automatically written to EEPROM.

Voltage Monitoring

The MAX16031 provides eight inputs, IN1–IN8, for voltage monitoring. The MAX16032 provides six inputs, IN1–IN6, for voltage monitoring. Each input voltage range is programmable through r17h[7:0] and r18h[7:0] (see Table 2). Voltage monitoring for each input is enabled through r1Ah[7:0] (see Table 2). There are four programmable thresholds per voltage monitor input: primary undervoltage, secondary undervoltage, primary overvoltage, and secondary overvoltage. All voltage thresholds are 8 bits wide. Only the 8 most significant bits of the conversion result are compared to the thresholds. See the *Miscellaneous Settings* section to set the amount of hysteresis for the thresholds. See Table 1 for an address map of all voltage monitor input threshold registers.

ADC inputs are configurable for two different modes: pseudo-differential and single-ended (see Table 3). In pseudo-differential mode, two inputs make up a differential pair. Psuedo-differential conversions are performed by taking a single-ended conversion at each input of a differential pair and then subtracting the results. The pseudo-differential mode is selectable for unipolar or bipolar operation. Unipolar differential operation allows only positive polarities of differential voltages. Bipolar differential operation allows negative and positive polarities of differential voltages. Bipolar conversions are in two's complement format. For example,

Table 2. Input Monitor Ranges and Enables

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
17h	97h	[1:0]	**IN1 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved
		[3:2]	**IN2 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved
		[5:4]	**IN3 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved
		[7:6]	**IN4 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved

Table 2. Input Monitor Ranges and Enables (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
18h	98h	[1:0]	**IN5 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved
		[3:2]	**IN6 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved
		[5:4]	**IN7 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved
		[7:6]	**IN8 Voltage Range Selection:** 00 = 5.6V, 01 = 2.8V 10 = 1.4V, 11 = Reserved
1Ah	9Ah	[0]	**IN1 Monitoring Enable:** 0 = IN1 monitoring disabled 1 = IN1 monitoring enabled
		[1]	**IN2 Monitoring Enable:** 0 = IN2 monitoring disabled 1 = IN2 monitoring enabled
		[2]	**IN3 Monitoring Enable:** 0 = IN3 monitoring disabled 1 = IN3 monitoring enabled
		[3]	**IN4 Monitoring Enable:** 0 = IN4 monitoring disabled 1 = IN4 monitoring enabled
		[4]	**IN5 Monitoring Enable:** 0 = IN5 monitoring disabled 1 = IN5 monitoring enabled
		[5]	**IN6 Monitoring Enable:** 0 = IN6 monitoring disabled 1 = IN6 monitoring enabled
		[6]	**IN7 Monitoring Enable:** 0 = IN7 monitoring disabled 1 = IN7 monitoring enabled
		[7]	**IN8 Monitoring Enable:** 0 = IN8 monitoring disabled 1 = IN8 monitoring enabled

a -1V differential input (range of 5.6V) gives a decimal code of -183, which is 1101001001 in two's complement binary form. In single-ended mode, conversions are performed between a single input and ground. When single-ended mode is selected, conversions are always unipolar regardless of r1Ch[7:4]. The single-ended and pseudo-differential ADC mode equations are shown below.

Unipolar single-ended mode:

$$X_{ADC} = INT\left(\frac{V_{IN-}}{V_{REF}} \times 1024\right)$$

where X_{ADC} is the resulting code in decimal, V_{IN} is the voltage at a voltage monitoring input, and V_{RANGE} is the selected range programmed in r17h and r18h.

Bipolar/unipolar pseudo-differential mode:

$$X_{ADC} = INT\left(\frac{V_{IN+}}{V_{REF}} \times 1024\right) - INT\left(\frac{V_{IN-}}{V_{REF}} \times 1024\right)$$

where X_{ADC} is the resulting code in decimal, V_{IN+} is the voltage at a positive input of a differential voltage monitoring input pair, V_{IN-} is the voltage at a negative input of a differential voltage monitoring input pair, and V_{RANGE} is the selected range programmed in r17h and r18h.

Table 3. IN1–IN8 ADC Input Mode Selection

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
1Ch	9Ch	[0]	**IN1/IN2 Single-Ended/Pseudo-Differential:** 0 = IN1 and IN2 conversions are single-ended. 1 = IN1 and IN2 conversions are pseudo-differential (IN1 to IN2).
		[1]	**IN3/IN4 Single-Ended/Pseudo-Differential:** 0 = IN3 and IN4 conversions are single-ended. 1 = IN3 and IN4 conversions are pseudo-differential (IN3 to IN4).
		[2]	**IN5/IN6 Single-Ended/Pseudo-Differential:** 0 = IN5 and IN6 conversions are single-ended. 1 = IN5 and IN6 conversions are pseudo-differential (IN5 to IN6).
		[3]	**IN7/IN8 Single-Ended/Pseudo-Differential:** 0 = IN7 and IN8 conversions are single-ended. 1 = IN7 and IN8 conversions are pseudo-differential (IN7 to IN8).
		[4]	**IN1/IN2 Unipolar/Bipolar:** 0 = IN1 and IN2 conversions are unipolar. 1 = IN1 and IN2 conversions are bipolar (two's complement).
		[5]	**IN3/IN4 Unipolar/Bipolar:** 0 = IN3 and IN4 conversions are unipolar. 1 = IN3 and IN4 conversions are bipolar (two's complement).
		[6]	**IN5/IN6 Unipolar/Bipolar:** 0 = IN5 and IN6 conversions are unipolar. 1 = IN5 and IN6 conversions are bipolar (two's complement).
		[7]	**IN7/IN8 Unipolar/Bipolar:** 0 = IN7 and IN8 conversions are unipolar. 1 = IN7 and IN8 conversions are bipolar (two's complement).

Current Monitoring

The MAX16031 provides current-sense inputs CS+/CS- and a current-sense amplifier for current monitoring (see Figure 3). There are two programmable current-sense thresholds: primary overcurrent and secondary overcurrent. For fast fault detection, the primary overcurrent threshold is implemented with an analog comparator connected to the $\overline{OVERC}$ output. The primary threshold equation is:

$$I_{TH} = \frac{V_{CSTH}}{R_{SENSE}}$$

where I_{TH} is the current threshold to be set, V_{CSTH} is the threshold set by r19h[1:0], and R_{SENSE} is the value of the sense resistor. See Table 4 for a description of r19h. The ADC output for a current-sense conversion is:

$$X_{ADC} = \frac{V_{SENSE} \times A_V}{V_{RBP}} \times \left(2^8 - 1\right)$$

where X_{ADC} is the 8-bit decimal ADC result, V_{SENSE} is $V_{CS+} - V_{CS-}$, A_V is the current-sense voltage gain set by r19h[1:0], and V_{RBP} is the reference voltage at RBP (1.4V typical).

$\overline{OVERC}$ is latched when the primary overcurrent threshold is exceeded by programming r5Ch[4]. The latch is cleared by writing a '1' to r53h[6]. $\overline{OVERC}$ depends only on the primary overcurrent threshold. Other fault outputs are programmed to depend on the secondary overcurrent threshold. The secondary overcurrent threshold is implemented through ADC conversions and digital comparisons. The secondary overcurrent threshold contains programmable time delay options located in r5Ch[1:0]. Primary and secondary current-sense faults are enabled/disabled through r1Bh[3].

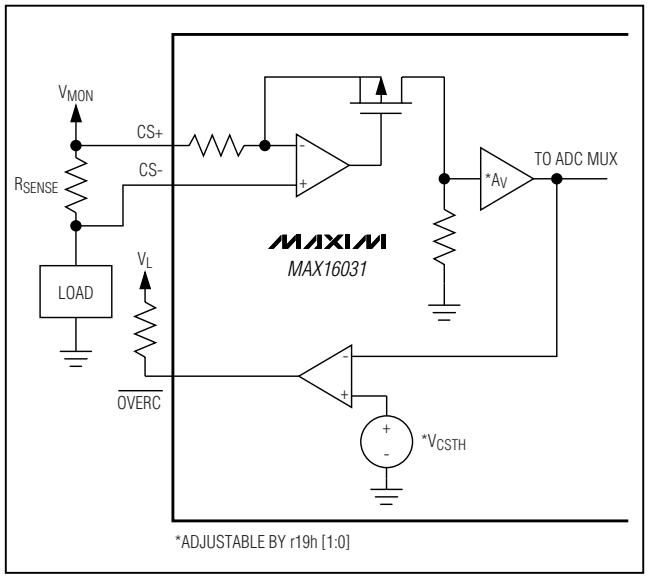


Figure 3. Current-Sense Block Diagram

Temperature Monitoring

The MAX16031 provides two sets of remote diode inputs, DXP1/DXN1 and DXP2/DXN2, and one internal temperature sensor. The MAX16032 provides one set, DXP1/DXN1, and one internal temperature sensor. Calibration registers provide adjustments for gain and offset to accommodate different types of remote diodes. The internal temperature sensor circuitry is factory trimmed. In addition to offset/gain trimming, a programmable lowpass filter is provided. See Figure 4 for the block diagram of the temperature sensor circuitry. The remote diode is actually a diode-connected transistor. See Application Notes AN1057 and AN1944 for information on error budget and several transistor manufacturers.

Table 4. Overcurrent Primary Threshold and Remote Temperature Sense Gain Trim

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
19h	99h	[1:0]	Overcurrent Primary Threshold and Current-Sense Gain Setting: 00 = 200mV threshold, A_V = 6V/V 01 = 100mV threshold, A_V = 12V/V 10 = 50mV threshold, A_V = 24V/V 11 = 25mV threshold, A_V = 48V/V
		[7:2]	Remote Temperature Sensor 1 Gain Trim. Note bit 6 is inverted.
4Fh	CFh	[5:0]	Remote Temperature Sensor 1 Gain Trim
		[7:6]	Not used

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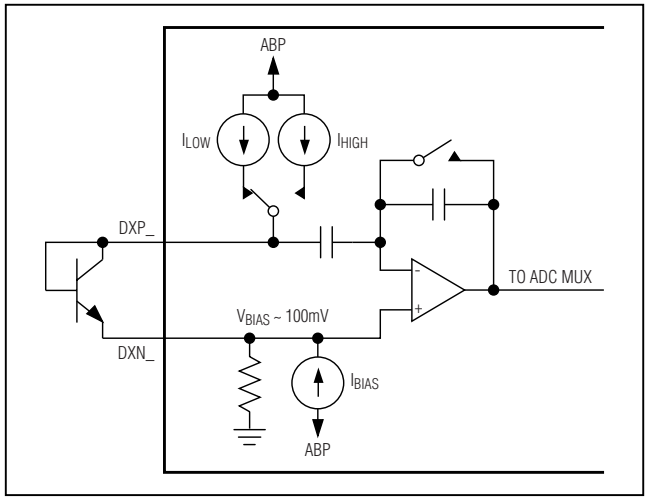

Figure 4. Remote Temperature Sensor Amplifier Circuitry

The ADC converts the internal sensor and remote sensor amplifier outputs. Each time the ADC converts all enabled parameters, the temperature conversions are compared to the temperature threshold registers (r46h to r4Bh and r4Dh). Unlike the voltage input comparators, the temperature threshold comparators are 10 bits wide. $\overline{OVERT}$ is the designated output for temperature faults, although other outputs are programmed to depend on temperature faults as well. See the *Programmable Inputs/Outputs* section for more information on programming output dependencies. See the *Faults* section for more information on setting temperature fault thresholds.

The remote temperature sensor amplifier detects a short or open between DXP_ and DXN_. The detection of these events is programmed to cause a fault. Temperature thresholds and conversions are in a two's complement temperature format, where 1 LSB corresponds to 0.5°C. The data format for temperature conversions is illustrated in Table 5.

Offset and gain errors for remote temperature sensor measurements are user-trimmed through gain registers r19h[7:2]/r4Fh[5:0] and offset registers r1Bh[7:5]/r4D[6:4], as shown in Tables 4 and 6. The gain value trims the high (56µA) drive current source to compensate for the n-factor of the remote diode. The offset value is multiplied by 4 and added to the conversion result numerically. The MAX16031/MAX16032 contain an internal lowpass filter at DXN_ and DXP_ to reduce noise. See the *Miscellaneous Settings* section for more information on programming the filter cutoff frequency.

Table 5. Temperature Data Format

TEMPERATURE (°C)	DIGITAL CODE
+128	1100000000
+125	1011111010
+100	1011010000
+25.5	1000110011
0	1000000000
-10	0111101100
-75	0101101010
-100	0100111000
-128	0100000000
Diode fault	0000000000

Reading ADC Results

ADC conversion results are read from the ADC conversion registers through the I²C/SMBus-compatible or JTAG interfaces (see Table 7). These registers are also used for fault threshold comparison. Voltage monitoring thresholds are compared with only the first 8 MSBs of the conversion results.

Programmable Inputs/Outputs

The MAX16031 provides two general fault outputs, $\overline{FAULT1}$ and $\overline{FAULT2}$, one reset output $\overline{RESET}$, one temperature fault output $\overline{OVERT}$, one current fault output $\overline{OVERC}$, two general-purpose inputs/outputs GPIO1 and GPIO2, and one SMBALERT#-compatible output $\overline{ALERT}$. The MAX16032 provides the same except $\overline{OVERC}$. All outputs are open drain and require pullup resistors. Fault outputs do not latch except for $\overline{OVERC}$, which either latches or does not latch depending on the configuration bit in r5Ch. Individual fault flag bits, however, latch (see the *Faults* section) and must be cleared one bit at a time by writing a byte containing all zeros except for a single '1' in the bit to be cleared.

The general outputs, $\overline{FAULT1}$ and $\overline{FAULT2}$, are identical in functionality and are programmed to depend on overvoltage, undervoltage, overtemperature, and overcurrent parameters. See r1Dh and r1Eh in Table 8 for more detailed information regarding the general fault output dependencies.

The reset output $\overline{RESET}$ provides many programmable output dependencies as well as reset timeouts. See r20h and r21h in Table 8 for detailed information on $\overline{RESET}$ output dependencies and timeouts.

The temperature fault output $\overline{OVERT}$ indicates temperature-related faults. $\overline{OVERT}$ is programmed to depend on any primary temperature threshold and/or the remote diode open/short flags. $\overline{OVERT}$ latches low dur-

Table 6. Temperature Sensor Fault Enable, Current-Sense Fault Enable, SMBALERT# Enable, and Temperature Offset Trim

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
1Bh	9Bh	[0]	**Internal Temperature Sensor Faults Enable:** 0 = Internal temperature sensor faults disabled 1 = Internal temperature sensor faults enabled
		[1]	**Remote Temperature Sensor 1 Faults Enable:** 0 = Remote temperature sensor 1 faults disabled 1 = Internal temperature sensor 1 faults enabled
		[2]	**Remote Temperature Sensor 2 Faults Enable:** 0 = Remote temperature sensor 2 faults disabled 1 = Remote temperature sensor 2 faults enabled
		[3]	**Current-Sense Fault Enable:** 0 = Current-sense faults disabled 1 = Current-sense faults enabled
		[4]	**SMBALERT# Enable ($\overline{\text{ALERT}}$):** 0 = SMBALERT# disabled 1 = SMBALERT# enabled
		[7:5]	**Remote Temperature Sensor 1 Offset Trim:** Offset = 4 × X, where X is the two's-complement 3-bit temperature code (1 LSB = 0.5°C). Since X is multiplied by 4, the offset LSB size is 2°C, allowing a total offset adjustment of ±6°C.
4Dh	CDh	[1:0]	Internal Temperature Sensor Primary Overtemperature Threshold LSB
		[3:2]	Internal Temperature Sensor Secondary Overtemperature Threshold LSB
		[6:4]	**Remote Temperature Sensor 2 Offset Trim:** Offset = 4 × X, where X is the two's-complement 3-bit temperature code (1 LSB = 0.5°C). Since X is multiplied by 4, the offset LSB size is 2°C, allowing a total offset adjustment of ±6°C.
		[7]	Not used.

ing diode open/short fault conditions, and the corresponding diode open/short flags must be cleared to release the latch. See r1Fh in Table 8 for more information on $\overline{\text{OVERT}}$ output dependencies.

The current fault output $\overline{\text{OVERC}}$ indicates overcurrent events. $\overline{\text{OVERC}}$ only depends on the primary analog overcurrent threshold. See the *Current Monitoring* section for more information about the current-sense amplifier and the primary threshold. The secondary overcurrent threshold is set digitally and is used by other outputs. The secondary threshold also has a programmable timeout option (see *Miscellaneous Settings* section).

GPIO1 and GPIO2 are programmable as logic inputs, manual reset inputs, logic outputs, or fault dependent outputs. See r22h–r25h in Table 8 for more detailed information on GPIO1/GPIO2 functionality. GPIO1 and GPIO2 assert low when configured as a fault output.

$\overline{\text{ALERT}}$ is an SMBALERT#-compatible fault interrupt output. When enabled, it is logically ANDed with outputs $\overline{\text{RESET}}$, $\overline{\text{FAULT1}}$, $\overline{\text{FAULT2}}$, $\overline{\text{OVERT}}$, $\overline{\text{OVERC}}$, and GPIO1/GPIO2 (only if enabled as fault outputs). When any fault output is asserted, $\overline{\text{ALERT}}$ also asserts, interrupting the SMBus master to query the fault. The master needs to answer MAX16031/MAX16032 with a specific SMBus command (ARA) to retrieve the slave address of the interrupting device. See the *I²C/SMBus-Compatible Serial Interface* section for more details.

Table 7. ADC Conversion Registers

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
00h	—	[7:0]	IN1 ADC Conversion Result (MSB)
01h	—	[1:0]	IN1 ADC Conversion Result (LSB)
		[7:2]	Reserved
02h	—	[7:0]	IN2 ADC Conversion Result (MSB)
03h	—	[1:0]	IN2 ADC Conversion Result (LSB)
		[7:2]	Reserved
04h	—	[7:0]	IN3 ADC Conversion Result (MSB)
05h	—	[1:0]	IN3 ADC Conversion Result (LSB)
		[7:2]	Reserved
06h	—	[7:0]	IN4 ADC Conversion Result (MSB)
07h	—	[1:0]	IN4 ADC Conversion Result (LSB)
		[7:2]	Reserved
08h	—	[7:0]	IN5 ADC Conversion Result (MSB)
09h	—	[1:0]	IN5 ADC Conversion Result (LSB)
		[7:2]	Reserved
0Ah	—	[7:0]	IN6 ADC Conversion Result (MSB)
0Bh	—	[1:0]	IN6 ADC Conversion Result (LSB)
		[7:2]	Reserved
0Ch	—	[7:0]	IN7 ADC Conversion Result (MSB)
0Dh	—	[1:0]	IN7 ADC Conversion Result (LSB)
		[7:2]	Reserved
0Eh	—	[7:0]	IN8 ADC Conversion Result (MSB)
0Fh	—	[1:0]	IN8 ADC Conversion Result (LSB)
		[7:2]	Reserved
10h	—	[7:0]	Internal Temperature Sensor ADC Conversion Result (MSB)
11h	—	[1:0]	Internal Temperature Sensor ADC Conversion Result (LSB)
		[7:2]	Reserved
12h	—	[7:0]	Remote Temperature Sensor 1 ADC Conversion Result (MSB)
13h	—	[1:0]	Remote Temperature Sensor 1 ADC Conversion Result (LSB)
		[7:2]	Reserved
14h	—	[7:0]	Remote Temperature Sensor 2 ADC Conversion Result (MSB)
15h	—	[1:0]	Remote Temperature Sensor 2 ADC Conversion Result (LSB)
		[7:2]	Reserved
16h	—	[7:0]	Current-Sense ADC Conversion Result

Table 8. Output Dependencies

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
1Dh	9Dh	[0]	1 = $\overline{\text{FAULT1}}$ depends on the secondary undervoltage thresholds of all enabled IN1–IN8.
		[1]	1 = $\overline{\text{FAULT1}}$ depends on the primary overvoltage thresholds of all enabled IN1–IN8.
		[2]	1 = $\overline{\text{FAULT1}}$ depends on the secondary overvoltage thresholds of all enabled IN1–IN8.
		[3]	1 = $\overline{\text{FAULT1}}$ depends on the secondary overtemperature threshold of the internal temperature sensor.
		[4]	1 = $\overline{\text{FAULT1}}$ depends on the secondary overtemperature threshold of remote temperature sensor 1.
		[5]	1 = $\overline{\text{FAULT1}}$ depends on the secondary overtemperature threshold of remote temperature sensor 2.
		[6]	1 = $\overline{\text{FAULT1}}$ depends on the secondary overcurrent threshold.
		[7]	Reserved
1Eh	9Eh	[0]	1 = $\overline{\text{FAULT2}}$ depends on the secondary undervoltage thresholds of all enabled IN1–IN8.
		[1]	1 = $\overline{\text{FAULT2}}$ depends on the primary overvoltage thresholds of all enabled IN1–IN8.
		[2]	1 = $\overline{\text{FAULT2}}$ depends on the secondary overvoltage thresholds of all enabled IN1–IN8.
		[3]	1 = $\overline{\text{FAULT2}}$ depends on the secondary overtemperature threshold of the internal temperature sensor.
		[4]	1 = $\overline{\text{FAULT2}}$ depends on the secondary overtemperature threshold of remote temperature sensor 1.
		[5]	1 = $\overline{\text{FAULT2}}$ depends on the secondary overtemperature threshold of remote temperature sensor 2.
		[6]	1 = $\overline{\text{FAULT2}}$ depends on the secondary overcurrent threshold.
		[7]	Reserved
1Fh	9Fh	[0]	1 = $\overline{\text{OVERT}}$ depends on the primary overtemperature threshold of the internal temperature sensor.
		[1]	1 = $\overline{\text{OVERT}}$ depends on the primary overtemperature threshold of the remote temperature sensor 1.
		[2]	1 = $\overline{\text{OVERT}}$ depends on the primary overtemperature threshold of the remote temperature sensor 2.

Table 8. Output Dependencies (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
1Fh	9Fh	[3]	1 = $\overline{\text{OVERT}}$ depends on the diode short flag of remote temperature sensor 1. $\overline{\text{OVERT}}$ latches when the diode is shorted. Clear the latch by writing to r50h.
		[4]	1 = $\overline{\text{OVERT}}$ depends on the diode open flag of remote temperature sensor 1. $\overline{\text{OVERT}}$ latches when the diode is open. Clear the latch by writing to r50h.
		[5]	1 = $\overline{\text{OVERT}}$ depends on the diode short flag of remote temperature sensor 2. $\overline{\text{OVERT}}$ latches when the diode is shorted. Clear the latch by writing to r50h.
		[6]	1 = $\overline{\text{OVERT}}$ depends on the diode open flag of remote temperature sensor 2. $\overline{\text{OVERT}}$ latches when the diode is open. Clear the latch by writing to r50h.
		[7]	Reserved
20h	A0h	[2:0]	**$\overline{\text{RESET}}$ Configuration:** 000 = $\overline{\text{RESET}}$ has no dependencies; asserts during boot and boot-up timeout and then deasserts indefinitely. 001 = $\overline{\text{RESET}}$ depends on the primary undervoltage thresholds at inputs that are selected by r21h[7:0]. 010 = $\overline{\text{RESET}}$ depends on the primary overvoltage thresholds at inputs that are selected by r21h[7:0]. 011 = $\overline{\text{RESET}}$ depends on both the primary undervoltage and overvoltage thresholds at those inputs that are selected by r21h[7:0]. 100 = $\overline{\text{RESET}}$ depends on the primary undervoltage thresholds at inputs that are selected by r21h[7:0] and the internal temperature sensor primary overtemperature threshold. 101 = $\overline{\text{RESET}}$ depends on both the primary undervoltage and overvoltage thresholds at those inputs that are selected by r21h[7:0] and the internal temperature sensor primary overtemperature threshold. 110 = $\overline{\text{RESET}}$ depends on the primary undervoltage thresholds at inputs that are selected by r21h[7:0] and each internal/remote temperature sensor primary overtemperature threshold. 111 = $\overline{\text{RESET}}$ depends on both the primary undervoltage and overvoltage thresholds at those inputs that are selected by r21h[7:0] and each internal/remote temperature sensor primary overtemperature threshold.
		[5:3]	**$\overline{\text{RESET}}$ Timeout:** 000 = 25µs 001 = 2.5ms 010 = 10ms 011 = 40ms 100 = 160ms 101 = 640ms 110 = 1280ms 111 = 2560ms
		[7:6]	Reserved

Table 8. Output Dependencies (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
21h	A1h	[0]	1 = $\overline{\text{RESET}}$ depends on IN1 with thresholds defined by r20h[2:0].
		[1]	1 = $\overline{\text{RESET}}$ depends on IN2 with thresholds defined by r20h[2:0].
		[2]	1 = $\overline{\text{RESET}}$ depends on IN3 with thresholds defined by r20h[2:0].
		[3]	1 = $\overline{\text{RESET}}$ depends on IN4 with thresholds defined by r20h[2:0].
		[4]	1 = $\overline{\text{RESET}}$ depends on IN5 with thresholds defined by r20h[2:0].
		[5]	1 = $\overline{\text{RESET}}$ depends on IN6 with thresholds defined by r20h[2:0].
		[6]	1 = $\overline{\text{RESET}}$ depends on IN7 with thresholds defined by r20h[2:0].
		[7]	1 = $\overline{\text{RESET}}$ depends on IN8 with thresholds defined by r20h[2:0].
22h	A2h	[2:0]	GPIO1 Output Dependencies: 000 = GPIO1 is a digital input that is read from r22h[7]. 001 = GPIO1 is a digital manual reset input that asserts $\overline{\text{RESET}}$ when asserted. The state of GPIO1 is read from r22h[7]. 010 = GPIO1 is a digital output that is written to through r22h[6]. 011 = GPIO1 is a digital fault output that depends on conditions selected by r23h[6:0]. 100 = GPIO1 is a digital output that depends on primary thresholds at the input selected by r22h[5:3]. 101 =GPIO1 is a digital output that depends on primary thresholds at the input selected by r22h[5:3] and on conditions selected by r23h[6:0]. 110 = Reserved 111 = Reserved
		[5:3]	GPIO1 Single-Input Primary Threshold Voltage Monitor (r22h[2:0] = 100 or 101 only). GPIO1 asserts low when any primary threshold of this input is exceeded: 000 = IN1 001 = IN2 010 = IN3 011 = IN4 100 = IN5 101 = IN6 110 = IN7 111 = IN8
		[6]	**GPIO1 Output (write to this bit):** 1 = GPIO1 is set high if GPIO1 is configured as an output. 0 = GPIO1 is set low if GPIO1 is configured as an output.
		[7]	**GPIO1 Input State (read from this bit):** 1 = Indicates that GPIO1 is high regardless if GPIO1 is set as an output or input. 0 = Indicates that GPIO1 is low regardless if GPIO1 is set as an output or input.

Table 8. Output Dependencies (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
23h	A3h	[0]	1 = GPIO1 depends on the secondary undervoltage thresholds of all enabled IN1–IN8.
		[1]	1 = GPIO1 depends on the primary overvoltage thresholds of all enabled IN1–IN8.
		[2]	1 = GPIO1 depends on the secondary overvoltage thresholds of all enabled IN1–IN8.
		[3]	1 = GPIO1 depends on the secondary overtemperature threshold of the internal temperature sensor.
		[4]	1 = GPIO1 depends on the secondary overtemperature threshold of remote temperature sensor 1.
		[5]	1 = GPIO1 depends on the secondary overtemperature threshold of remote temperature sensor 2.
		[6]	1 = GPIO1 depends on the secondary overcurrent threshold.
		[7]	Reserved
24h	A4h	[2:0]	**GPIO2 Output Dependencies:** 000 = GPIO2 is a digital input that is read from r24h[7]. 001 = GPIO2 is a digital manual reset input that asserts $\overline{\text{RESET}}$ when asserted. The state of GPIO2 is read from r24h[7]. 010 = GPIO2 is a digital output that is written to through r24h[6]. 011 = GPIO2 is a digital fault output that depends on conditions selected by r25h[6:0]. 100 = GPIO2 is a digital output that depends on primary thresholds at the input selected by r24h[5:3]. 101 = GPIO2 is a digital output that depends on primary thresholds at the input selected by r24h[5:3] and on conditions selected by r25h[6:0]. 110 = Reserved 111 = Reserved
		[5:3]	**GPIO2** Single-Input Primary Threshold Voltage Monitor (r24h[2:0] = 100 or 101 only). **GPIO2** asserts low when the primary threshold of this input is exceeded: 000 = IN1 001 = IN2 010 = IN3 011 = IN4 100 = IN5 101 = IN6 110 = IN7 111 = IN8
		[6]	**GPIO2 Output (write to this bit):** 1 = GPIO2 is set high if GPIO2 is configured as an output. 0 = GPIO2 is set low if GPIO2 is configured as an output.
		[7]	**GPIO2 Input (read from this bit):** 1 = Indicates that GPIO2 is high regardless if GPIO2 is set as an output or input. 0 = Indicates that GPIO2 is low regardless if GPIO2 is set as an output or input.

Table 8. Output Dependencies (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
25h	A5h	[0]	1 = GPIO2 depends on the secondary undervoltage thresholds of all enabled IN1–IN8.
		[1]	1 = GPIO2 depends on the primary overvoltage thresholds of all enabled IN1–IN8.
		[2]	1 = GPIO2 depends on the secondary overvoltage thresholds of all enabled IN1–IN8.
		[3]	1 = GPIO2 depends on the secondary overtemperature threshold of the internal temperature sensor.
		[4]	1 = GPIO2 depends on the secondary overtemperature threshold of remote temperature sensor 1.
		[5]	1 = GPIO2 depends on the secondary overtemperature threshold of remote temperature sensor 2.
		[6]	1 = GPIO2 depends on the secondary overcurrent threshold.
		[7]	Reserved

Faults

The MAX16031/MAX16032 offer many configurable options for detecting and managing system faults. Fault thresholds are set in r26h–r4Eh, as shown in Table 9. Any threshold that is configured to cause a fault can be masked at any time from causing a fault by setting bits in r54h–r57h, as shown in Table 10. Fault flags indicate the fault status of a particular input. The fault flag of any monitored input in the device can be read at any time from r50h–r53h, as shown in Table 11. Clear a fault flag by writing a '1' to the appropriate bit in the flag register.

Table 9. Fault Thresholds

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
26h	A6h	[7:0]	IN1 Primary Undervoltage Threshold
27h	A7h	[7:0]	IN1 Primary Overvoltage Threshold
28h	A8h	[7:0]	IN1 Secondary Undervoltage Threshold
29h	A9h	[7:0]	IN1 Secondary Overvoltage Threshold
2Ah	AAh	[7:0]	IN2 Primary Undervoltage Threshold
2Bh	ABh	[7:0]	IN2 Primary Overvoltage Threshold
2Ch	ACh	[7:0]	IN2 Secondary Undervoltage Threshold
2Dh	ADh	[7:0]	IN2 Secondary Overvoltage Threshold
2Eh	AEh	[7:0]	IN3 Primary Undervoltage Threshold
2Fh	AFh	[7:0]	IN3 Primary Overvoltage Threshold
30h	B0h	[7:0]	IN3 Secondary Undervoltage Threshold
31h	B1h	[7:0]	IN3 Secondary Overvoltage Threshold
32h	B2h	[7:0]	IN4 Primary Undervoltage Threshold
33h	B3h	[7:0]	IN4 Primary Overvoltage Threshold

Table 9. Fault Thresholds (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
34h	B4h	[7:0]	IN4 Secondary Undervoltage Threshold
35h	B5h	[7:0]	IN4 Secondary Overvoltage Threshold
36h	B6h	[7:0]	IN5 Primary Undervoltage Threshold
37h	B7h	[7:0]	IN5 Primary Overvoltage Threshold
38h	B8h	[7:0]	IN5 Secondary Undervoltage Threshold
39h	B9h	[7:0]	IN5 Secondary Overvoltage Threshold
3Ah	BAh	[7:0]	IN6 Primary Undervoltage Threshold
3Bh	BBh	[7:0]	IN6 Primary Overvoltage Threshold
3Ch	BCh	[7:0]	IN6 Secondary Undervoltage Threshold
3Dh	BDh	[7:0]	IN6 Secondary Overvoltage Threshold
3Eh	BEh	[7:0]	IN7 Primary Undervoltage Threshold
3Fh	BFh	[7:0]	IN7 Primary Overvoltage Threshold
40h	C0h	[7:0]	IN7 Secondary Undervoltage Threshold
41h	C1h	[7:0]	IN7 Secondary Overvoltage Threshold
42h	C2h	[7:0]	IN8 Primary Undervoltage Threshold
43h	C3h	[7:0]	IN8 Primary Overvoltage Threshold
44h	C4h	[7:0]	IN8 Secondary Undervoltage Threshold
45h	C5h	[7:0]	IN8 Secondary Overvoltage Threshold
46h	C6h	[7:0]	Internal Temperature Sensor Primary Overtemperature Threshold MSB (2 LSBs are in r4Dh[1:0]).
47h	C7h	[7:0]	Internal Temperature Sensor Secondary Overtemperature Threshold MSB (2 LSBs are in r4Dh[3:2]).
48h	C8h	[7:0]	Remote Temperature Sensor 1 Primary Overtemperature Threshold MSB (2 LSBs are in r4Eh[1:0]).
49h	C9h	[7:0]	Remote Temperature Sensor 1 Secondary Overtemperature Threshold MSB (2 LSBs are in r4Eh[3:2]).
4Ah	CAh	[7:0]	Remote Temperature Sensor 2 Primary Overtemperature Threshold MSB (2 LSBs are in r4Eh[5:4]).
4Bh	CBh	[7:0]	Remote Temperature Sensor 2 Secondary Overtemperature Threshold MSB (2 LSBs are in r4Eh[7:6]).
4Ch	CCh	[7:0]	Current-Sense Secondary Threshold
4Dh	CDh	[1:0]	Internal Temperature Sensor Primary Overtemperature Threshold LSB
		[3:2]	Internal Temperature Sensor Secondary Overtemperature Threshold LSB
		[6:4]	Remote Temperature Sensor 2, Offset Trim
		[7]	Not used
4Eh	CEh	[1:0]	Remote Temperature Sensor 1 Primary Overtemperature Threshold LSB
		[3:2]	Remote Temperature Sensor 1 Secondary Overtemperature Threshold LSB
		[5:3]	Remote Temperature Sensor 2 Primary Overtemperature Threshold LSB
		[7:6]	Remote Temperature Sensor 2 Secondary Overtemperature Threshold LSB

Table 10. Fault Masks

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
54h	D4h	[0]	1 = Short-circuit detection at remote temperature sensor 1 is masked.
		[1]	1 = Open-circuit detection at remote temperature sensor 1 is masked.
		[2]	1 = Short-circuit detection at remote temperature sensor 2 is masked.
		[3]	1 = Open-circuit detection at remote temperature sensor 2 is masked.
		[7:4]	Not used.
55h	D5h	[0]	1 = IN1 primary overvoltage and undervoltage faults are masked.
		[1]	1 = IN2 primary overvoltage and undervoltage faults are masked.
		[2]	1 = IN3 primary overvoltage and undervoltage faults are masked.
		[3]	1 = IN4 primary overvoltage and undervoltage faults are masked.
		[4]	1 = IN5 primary overvoltage and undervoltage faults are masked.
		[5]	1 = IN6 primary overvoltage and undervoltage faults are masked.
		[6]	1 = IN7 primary overvoltage and undervoltage faults are masked.
		[7]	1 = IN8 primary overvoltage and undervoltage faults are masked.
56h	D6h	[0]	1 = IN1 secondary overvoltage and undervoltage faults are masked.
		[1]	1 = IN2 secondary overvoltage and undervoltage faults are masked.
		[2]	1 = IN3 secondary overvoltage and undervoltage faults are masked.
		[3]	1 = IN4 secondary overvoltage and undervoltage faults are masked.
		[4]	1 = IN5 secondary overvoltage and undervoltage faults are masked.
		[5]	1 = IN6 secondary overvoltage and undervoltage faults are masked.
		[6]	1 = IN7 secondary overvoltage and undervoltage faults are masked.
		[7]	1 = IN1 secondary overvoltage and undervoltage faults are masked.
57h	D7h	[0]	1 = Internal temperature sensor primary overtemperature fault masked.
		[1]	1 = Remote temperature sensor 1 primary overtemperature fault masked.
		[2]	1 = Remote temperature sensor 2 primary overtemperature fault masked.
		[3]	1 = Internal temperature sensor secondary overtemperature fault masked.
		[4]	1 = Remote temperature sensor 1 secondary overtemperature fault masked.
		[5]	1 = Remote temperature sensor 2 secondary overtemperature fault masked.
		[6]	1 = Current-sense primary overcurrent fault masked.
		[7]	1 = Current-sense secondary overcurrent fault masked.

Table 11. Fault Flags

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
50h	D0h	[0]	1 = Short circuit detected at remote temperature sensor 1.
		[1]	1 = Open circuit detected at remote temperature sensor 1.
		[2]	1 = Short circuit detected at remote temperature sensor 2.
		[3]	1 = Open circuit detected at remote temperature sensor 2.
		[7:4]	Not used.
51h	D1h	[0]	1 = IN1 conversion result exceeds primary overvoltage or undervoltage thresholds.
		[1]	1 = IN2 conversion result exceeds primary overvoltage or undervoltage thresholds.
		[2]	1 = IN3 conversion result exceeds primary overvoltage or undervoltage thresholds.
		[3]	1 = IN4 conversion result exceeds primary overvoltage or undervoltage thresholds.
		[4]	1 = IN5 conversion result exceeds primary overvoltage or undervoltage thresholds.
		[5]	1 = IN6 conversion result exceeds primary overvoltage or undervoltage thresholds.
		[6]	1 = IN7 conversion result exceeds primary overvoltage or undervoltage thresholds.
		[7]	1 = IN8 conversion result exceeds primary overvoltage or undervoltage thresholds.
52h	D2h	[0]	1 = IN1 conversion result exceeds secondary overvoltage or undervoltage thresholds.
		[1]	1 = IN2 conversion result exceeds secondary overvoltage or undervoltage thresholds.
		[2]	1 = IN3 conversion result exceeds secondary overvoltage or undervoltage thresholds.
		[3]	1 = IN4 conversion result exceeds secondary overvoltage or undervoltage thresholds.
		[4]	1 = IN5 conversion result exceeds secondary overvoltage or undervoltage thresholds.
		[5]	1 = IN6 conversion result exceeds secondary overvoltage or undervoltage thresholds.
		[6]	1 = IN7 conversion result exceeds secondary overvoltage or undervoltage thresholds.
		[7]	1 = IN8 conversion result exceeds secondary overvoltage or undervoltage thresholds.
53h	D3h	[0]	1 = Internal temperature sensor conversion exceeds its primary overtemperature threshold.
		[1]	1 = Remote temperature sensor 1 conversion exceeds its primary overtemperature threshold.
		[2]	1 = Remote temperature sensor 2 conversion exceeds its primary overtemperature threshold.
		[3]	1 = Internal temperature sensor conversion exceeds its secondary overtemperature threshold.
		[4]	1 = Remote temperature sensor 1 conversion exceeds its secondary overtemperature threshold.
		[5]	1 = Remote temperature sensor 2 conversion exceeds its secondary overtemperature threshold.
		[6]	1 = Current-sense conversion exceeds its primary overcurrent threshold.
		[7]	1 = Current-sense conversion exceeds its secondary overcurrent threshold.

Table 12. Fault Log Dependency

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
58h	D8h	[0]	1 = Fault log triggered when IN1 is below its primary undervoltage threshold.
		[1]	1 = Fault log triggered when IN2 is below its primary undervoltage threshold.
		[2]	1 = Fault log triggered when IN3 is below its primary undervoltage threshold.
		[3]	1 = Fault log triggered when IN4 is below its primary undervoltage threshold.
		[4]	1 = Fault log triggered when IN5 is below its primary undervoltage threshold.
		[5]	1 = Fault log triggered when IN6 is below its primary undervoltage threshold.
		[6]	1 = Fault log triggered when IN7 is below its primary undervoltage threshold.
		[7]	1 = Fault log triggered when IN8 is below its primary undervoltage threshold.
59h	D9h	[0]	1 = Fault log triggered when IN1 is above its primary overvoltage threshold.
		[1]	1 = Fault log triggered when IN2 is above its primary overvoltage threshold.
		[2]	1 = Fault log triggered when IN3 is above its primary overvoltage threshold.
		[3]	1 = Fault log triggered when IN4 is above its primary overvoltage threshold.
		[4]	1 = Fault log triggered when IN5 is above its primary overvoltage threshold.
		[5]	1 = Fault log triggered when IN6 is above its primary overvoltage threshold.
		[6]	1 = Fault log triggered when IN7 is above its primary overvoltage threshold.
		[7]	1 = Fault log triggered when IN8 is above its primary overvoltage threshold.
5Ah	DAh	[0]	1 = Fault log triggered when current sense is above its primary overcurrent threshold.
		[1]	1 = Fault log triggered when internal temperature sensor is above its overtemperature threshold.
		[2]	1 = Fault log triggered when remote temperature sensor 1 is above its overtemperature threshold.
		[3]	1 = Fault log triggered when remote temperature sensor 2 is above its overtemperature threshold.
		[7:4]	Not used.

Fault Logging

If a specific input threshold is critical to the operation of the system, an automatic fault log is configured to trigger a transfer of fault information to EEPROM. The fault log dependencies are configured through r58h–r5Ah, as shown in Table 12. Logged fault information is read from EEPROM locations r80h–r8Eh, as shown in Table 13. Once a fault log event occurs, the fault log feature is locked and must be reset to enable a new fault log to be stored. Write a '1' to r5Fh[1] to reset the fault log. Fault information always contains the fault flag registers and is configured to also include the ADC result registers through r5Ch[7] (see the *Miscellaneous Settings* section). All stored ADC results are the 8 MSBs of the result.

Miscellaneous Settings

Table 14 shows several miscellaneous programmable items. Register r5Bh contains boot-up timeout and remote temperature sensor filter cutoff settings. Register r5Ch[1:0] sets the secondary overcurrent threshold timeout, which is the amount of delay after an overcurrent condition before the overcurrent condition becomes a fault. All voltage thresholds include two selectable hysteresis options programmed by r5Ch[5]. When r5Ch[6] = 1, the conditions programmed to cause a fault log event must happen for two consecutive ADC cycles rather than just one to provide an improvement in noise immunity. Register r5Ch[7] controls whether the ADC result registers are stored in EEPROM after a fault log. Register r5Eh provides storage space for a user-defined configuration or firmware version number. Register r5Fh[0] locks and unlocks the EEPROM and register set. Register r5Fh[1] indicates whether a fault log event occurred and the corresponding fault information is locked in EEPROM. Further fault log conditions will not write new fault information to the fault EEPROM until a '1' is written to r5Fh[1].

Table 13. Fault Log EEPROM

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
—	80h	[7:0]	Copy of r51h[7:0] at the time the fault log was triggered.
—	81h	[7:0]	Copy of r52h[7:0] at the time the fault log was triggered.
—	82h	[7:0]	Copy of r53h[7:0] at the time the fault log was triggered.
—	83h	[7:0]	IN1 conversion result at the time the fault log was triggered.
—	84h	[7:0]	IN2 conversion result at the time the fault log was triggered. 8 MSBs only.
—	85h	[7:0]	IN3 conversion result at the time the fault log was triggered. 8 MSBs only.
—	86h	[7:0]	IN4 conversion result at the time the fault log was triggered. 8 MSBs only.
—	87h	[7:0]	IN5 conversion result at the time the fault log was triggered. 8 MSBs only.
—	88h	[7:0]	IN6 conversion result at the time the fault log was triggered. 8 MSBs only.
—	89h	[7:0]	IN7 conversion result at the time the fault log was triggered. 8 MSBs only.
—	8Ah	[7:0]	IN8 conversion result at the time the fault log was triggered. 8 MSBs only.
—	8Bh	[7:0]	Internal temperature sensor conversion result at the time the fault log was triggered. 8 MSBs from 10-bit ADC conversion.
—	8Ch	[7:0]	Remote temperature sensor 1 conversion result at the time the fault log was triggered. 8 MSBs from 10-bit ADC conversion.
—	8Dh	[7:0]	Remote temperature sensor 2 conversion result at the time the fault log was triggered. 8 MSBs from 10-bit ADC conversion.
—	8Eh	[7:0]	Current-sense conversion result at the time the fault log was triggered.

I²C/SMBus-Compatible Serial Interface

The MAX16031/MAX16032 feature an I²C/SMBus-compatible 2-wire (SDA and SCL) serial interface for communication with a master device. All possible communication formats are shown in Figure 5. The slave address and SMBALERT# are described further in the following subsections. Figure 1 shows a detailed 2-wire interface timing diagram. For descriptions of the I²C and SMBus protocol and terminology, refer to the I²C-Bus Specification Version 2.1 and the System Management Bus (SMBus) Specification Version 2.0. The MAX16031/MAX16032 allow 2-wire communication up to 400kHz. SDA and SCL require external pullup resistors.

Slave Address

The slave address inputs, A0 and A1, are each capable of detecting three different states, allowing nine identical devices to share the same serial bus. Connect A0 and A1 to GND, DBP, or leave as not connected (N.C.). See Table 15 for a listing of all possible 7-bit address input connections and their corresponding serial-bus addresses.

SMBALERT#

SMBALERT# is an optional interrupt signal defined in Appendix A of the SMBus Specification. The MAX16031/MAX16032 provide output $\overline{ALERT}$ as this interrupt signal. If enabled, $\overline{ALERT}$ asserts if any one of the following outputs asserts: $\overline{FAULT1}$, $\overline{FAULT2}$, $\overline{RESET}$, $\overline{OVERT}$, or $\overline{OVERC}$. Additionally, if a GPIO_ is configured for a fault output, a fault at this output also causes $\overline{ALERT}$ to assert. $\overline{ALERT}$ deasserts when all fault conditions are removed (i.e., when all fault outputs are high).

Typically $\overline{ALERT}$ is connected to all other SMBALERT# open-drain signals in the system, creating a wired-OR function with all SMBALERT# outputs. When the master is interrupted by its SMBALERT# input, it stops or finishes the current bus transfer and places an alert response address (ARA) on the bus. The slave that pulled the SMBALERT# signal low acknowledges the ARA and places its own address on the bus, identifying itself to the master as the slave that caused the interrupt. The 7-bit ARA is '0001100' and the R/$\overline{W}$ bit is a don't care.

Send Byte Format

S	ADDRESS	R/$\overline{W}$	ACK	COMMAND	ACK	P
↓	7 bits	0		8 bits		↑

Slave Address: Address of the slave on the serial interface bus.

Data Byte: Presets the internal address pointer or represents a command.

Receive Byte Format

S	ADDRESS	R/$\overline{W}$	ACK	DATA	NACK	P
↓	7 bits	1		8 bits		↑

Slave Address: Address of the slave on the serial interface bus.

Data Byte: Data is read from the location pointed to by the internal address pointer.

Write Byte Format

S	ADDRESS	R/$\overline{W}$	ACK	COMMAND	ACK	DATA	ACK	P
↓	7 bits	0		8 bits		8 bits		↑

Slave Address: Address of the slave on the serial interface bus.

Command Byte: Sets the internal address pointer.

Data Byte: Data is written to the locations set by the internal address pointer.

SMBALERT#

S	ADDRESS	R/$\overline{W}$	ACK	DATA	NACK	P
↓	0001100	D.C.		8 bits		↑

Alert Response Address: Only the device that interrupted the master responds to this address.

Slave Address: Slave places its own address on the serial bus.

Read Byte Format

S	SLAVE ADDRESS	R/$\overline{W}$	ACK	COMMAND	ACK	SR	SLAVE ADDRESS	R/$\overline{W}$	ACK	DATA BYTE	NACK	P
↓	7 bits	0		8 bits		↓	7 bits	1		8 bits		↑

Slave Address: Address of the slave on the serial interface bus.

Command Byte: Sets the internal address pointer.

Data Byte: Data is written to the locations set by the internal address pointer.

Block Write Format

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	BYTE COUNT = N	ACK	DATA BYTE 1	ACK	DATA BYTE …	ACK	DATA BYTE N	ACK	P
↓	7 bits	0		8 bits		8 bits		8 bits		8 bits		8 bits		↑

Slave Address: Address of the slave on the serial interface bus.

Command Byte: FAh

Data Byte: Data is written to the locations set by the internal address pointer.

Slave to master

Master to slave

Block Read Format

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	SR	ADDRESS	$\overline{WR}$	ACK	BYTE COUNT = N	ACK	DATA BYTE N	ACK	DATA BYTE …	ACK	DATA BYTE N	NACK	P
↓	7 bits	0		8 bits		↓	7 bits	1		8 bits		8 bits		8 bits		8 bits		↑

Slave Address: Address of the slave on the serial interface bus.

Command Byte: FBh

Slave Address: Address of the slave on the serial interface bus.

Data Byte: Data is read from the locations set by the internal address pointer.

S = START Condition
P = STOP Condition
Sr = Repeated START Condition
D.C. = Don't Care

ACK = Acknowledge, SDA pulled low during rising edge of SCL.
NACK = Not acknowledge, SDA left high during rising edge of SCL.

All data is clocked in/out of the device on rising edges of SCL.

↓ = SDA transitions from high to low during period of SCL.

↑ = SDA transitions from low to high during period of SCL.

Figure 5. Communication Formats

Table 14. Miscellaneous Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
5Bh	DBh	[3:0]	**Postboot Timeout (all faults and outputs masked):** 0h = No timeout 1h = 0.974ms 2h = 2.030ms 3h = 3.978ms 4h = 8.038ms 5h = 15.99ms 6h = 31.99ms 7h = 63.99ms 8h = 128ms 9h = 256.0ms Ah = 512ms Bh = 1024ms Ch = 2048ms Dh = 4096ms Eh = 8192ms Fh = 16384ms
		[6:4]	**Temperature Sensor Lowpass Filter Cutoff:** 000 = No filter 001 = 2.53Hz 010 = 5.06Hz 011 = 10.1Hz 100 = 20.2Hz 101 = 40.5Hz 110 = 81Hz 111 = 162Hz
		[7]	Not used.
5Ch	DCh	[1:0]	**Overcurrent Secondary Threshold Timeout:** 00 = No delay 01 = 3.98ms 10 = 16ms 11 = 64ms
		[2]	**Latch $\overline{\text{OVERC}}$:** 0 = No latch 1 = Latched after assertion
		[4:3]	Not used.
		[5]	**Threshold Hysteresis (all thresholds):** 0 = 0.78% 1 = 1.17%

Table 14. Miscellaneous Settings (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
5Ch	DCh	[6]	**Consecutive Faults on Primary Thresholds:** 0 = Fault occurs after primary threshold is exceeded one time (normal operation). 1 = Fault occurs after primary threshold is exceeded twice.
		[7]	**Fault Log ADC Conversions Option:** 0 = When a fault log is triggered, only fault flags are saved in EEPROM. 1 = When a fault log is triggered, fault flags and ADC conversion results (8 MSBs) are saved in EEPROM.
5Eh	DEh	[7:0]	Firmware Version. 8 bits of memory for user-defined firmware version number.
5Fh	DFh	[0]	**Configuration Lock:** Write a '1' to r5Fh[0] to toggle this register bit. 0 = Register and EEPROM configuration unlocked. 1 = Register and EEPROM configuration locked.
		[1]	**Fault Log EEPROM Lock Flag (set automatically after fault log is triggered):** Write a '1' to r5Fh[1] to toggle this register bit. 0 = EEPROM is not locked. A triggered fault log stores fault information to EEPROM. 1 = A fault log has been triggered. Write a '1' to this bit to clear the flag and allow a new fault log to be triggered.
		[7:2]	Not used.

Table 15. Setting the I²C/SMBus Slave Address

A1	A0	BUS ADDRESS
GND	GND	0011000
GND	N.C.	0011001
GND	DBP	0011010
N.C.	GND	0101001
N.C.	N.C.	0101010
N.C.	DBP	0101011
DBP	GND	1001100
DBP	N.C.	1001111
DBP	DBP	1001110

Special Commands

The MAX16031/MAX16032 provide software reboot and fault log commands. A software reboot initiates the boot-up sequence, which normally occurs at POR. During boot-up, EEPROM configuration data is copied to registers. To initiate a software reboot, send 0xFC using the send byte format. A software-initiated fault log is functionally the same as a hardware-initiated fault log. During a fault log, ADC registers and fault information are logged in EEPROM. To trigger a software initiated fault log, send 0xFD using the send byte format.

JTAG Serial Interface

The MAX16031/MAX16032 contain an IEEE 1149.1- compliant JTAG port in addition to the I²C/SMBus-compatible serial bus. Either interface may be used to access internal memory; however, only one interface is allowed to run at a time. All digital I/Os on the MAX16031/MAX16032 are IEEE 1149.1 boundary-scan compliant, and contain the typical JTAG boundary scan cells that allow the inputs/outputs to be polled or forced high/low using standard JTAG instructions. The MAX16031/MAX16032 contain extra JTAG instructions and registers not included in the JTAG specification that provide access to internal memory. The extra instructions are: LOAD ADDRESS, WRITE, READ, REBOOT, SAVE, and USERCODE. The extra registers are: memory address, memory write, memory read, and user-code data. See Figure 6 for a block diagram of the JTAG interface.

Test Access Port (TAP) Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at TMS on the rising edge of TCK. See Figure 7 for a diagram of the finite state machine.

Test-Logic-Reset: At power-up, the TAP controller is in the test-logic-reset state. The instruction register contains the IDCODE instruction. All system logic of the device operates normally.

EEPROM-Based System Monitors with Nonvolatile Fault Memory

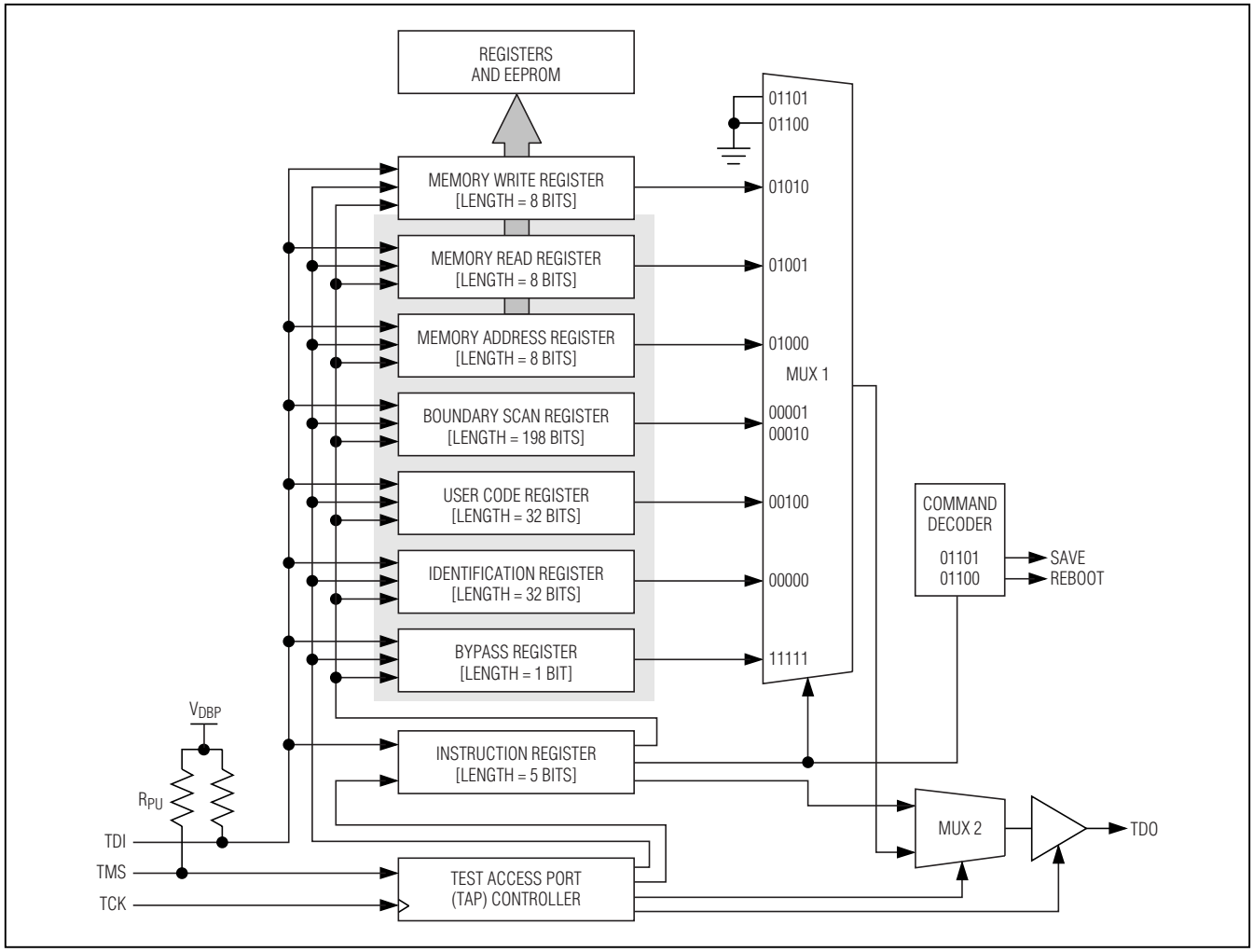

Figure 6. JTAG Block Diagram

Run-Test/Idle: The run-test/idle state is used between scan operations or during specific tests. The instruction register and test data registers remain idle.

Select-DR-Scan: All test data registers retain their previous state. With TMS low, a rising edge of TCK moves the controller into the capture-DR state and initiates a scan sequence. TMS high during a rising edge on TCK moves the controller to the select-IR-scan state.

Capture-DR: Data are parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected test data register does not allow parallel loads, the test data register remains at its current value. On the rising edge of TCK, the controller goes to the shift-DR state if TMS is low or it goes to the exit1-DR state if TMS is high.

Shift-DR: The test data register selected by the current instruction is connected between TDI and TDO and shifts data one stage toward its serial output on each rising edge of TCK while TMS is low. On the rising edge of TCK, the controller goes to the exit1-DR state if TMS is high.

Exit1-DR: While in this state, a rising edge on TCK puts the controller in the update-DR state. A rising edge on TCK with TMS low puts the controller in the pause-DR state.

Pause-DR: Shifting of the test data registers is halted while in this state. All test data registers retain their previous state. The controller remains in this state while TMS is low. A rising edge on TCK with TMS high puts the controller in the exit2-DR state.

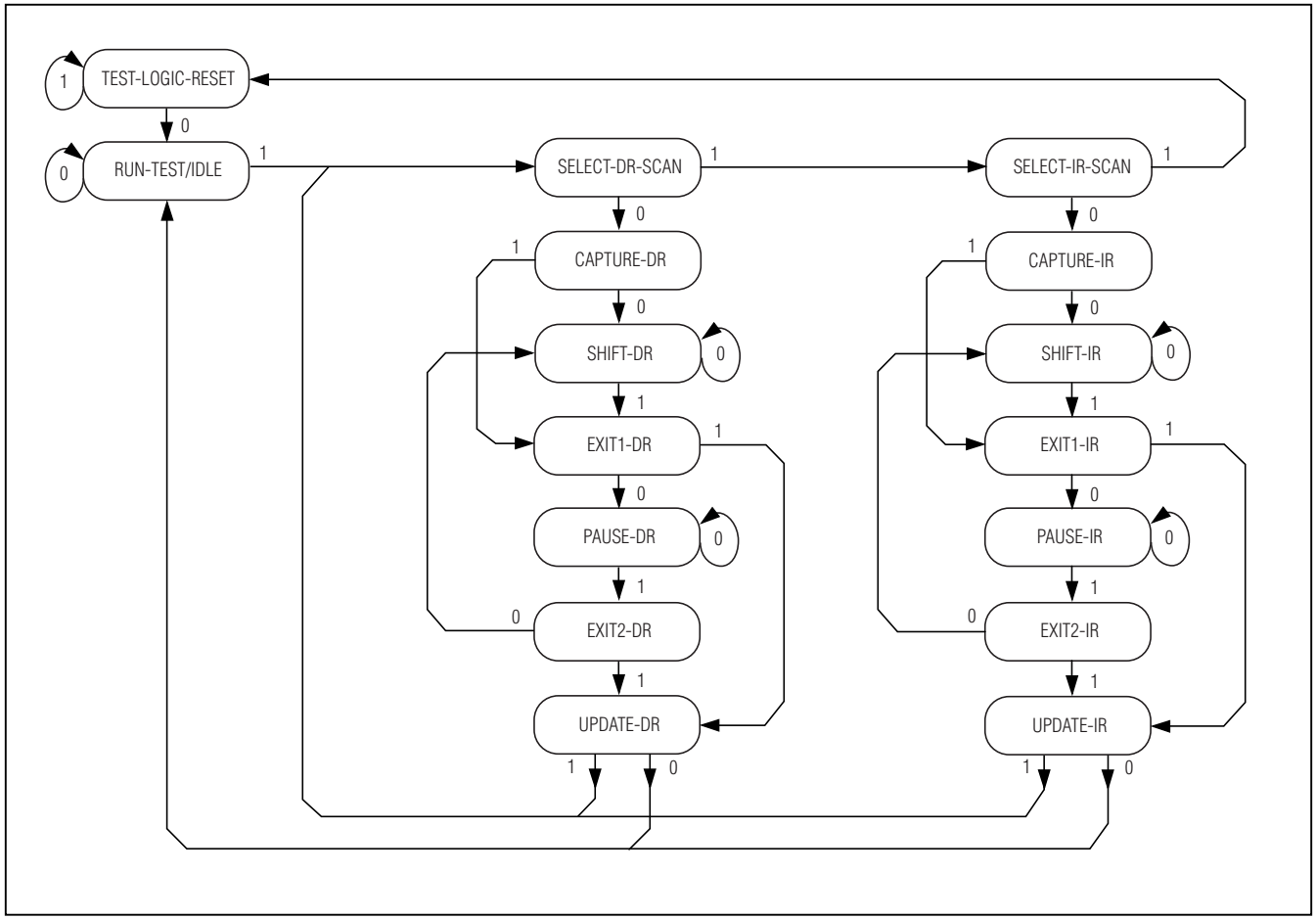

Figure 7. TAP Controller State Diagram

Exit2-DR: A rising edge on TCK with TMS high while in this state puts the controller in the update-DR state. A rising edge on TCK with TMS low enters the Shift-DR state.

Update-DR: A falling edge on TCK while in the update-DR state latches the data from the shift register path of the test data registers into a set of output latches. This prevents changes at the parallel output because of changes in the shift register. On the rising edge of TCK, the controller goes to the run-test/idle state if TMS is low or it goes to the select-DR-scan state if TMS is high.

Select-IR-Scan: All test data registers retain their previous state. The instruction register remains unchanged during this state. With TMS low, a rising edge on TCK moves the controller into the capture-IR state. TMS high during a rising edge on TCK puts the controller back into the test-logic-reset state.

Capture-IR: Use the capture-IR state to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of TCK. If TMS is high on the rising edge of TCK, the controller enters the exit1-IR state. If TMS is low on the rising edge of TCK, the controller enters the shift-IR state.

Shift-IR: In this state, the shift register in the instruction register is connected between TDI and TDO and shifts data one stage for every rising edge of TCK toward the TDO serial output while TMS is low. The parallel outputs of the instruction register as well as all test data registers remain at their previous states. A rising edge on TCK with TMS high moves the controller to the exit1-IR state. A rising edge on TCK with TMS low keeps the controller in the shift-IR state while moving data one stage through the instruction shift register.

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Exit1-IR: A rising edge on TCK with TMS low puts the controller in the pause-IR state. If TMS is high on the rising edge of TCK, the controller enters the update-IR state.

Pause-IR: Shifting of the instruction shift register is halted temporarily. With TMS high, a rising edge on TCK puts the controller in the exit2-IR state. The controller remains in the pause-IR state if TMS is low during a rising edge on TCK.

Exit2-IR: A rising edge on TCK with TMS high puts the controller in the update-IR state. The controller loops back to shift-IR if TMS is low during a rising edge of TCK in this state.

Update-IR: The instruction code that has been shifted into the instruction shift register is latched to the parallel outputs of the instruction register on the falling edge of TCK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on TCK with TMS low puts the controller in the run-test/idle state. With TMS high, the controller enters the select-DR-scan state.

Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 5 bits in length. When the TAP controller enters the shift-IR state, the instruction shift register is connected between TDI and TDO. While in the shift-IR state, a rising edge on TCK with TMS low shifts the data one stage toward the serial output at TDO. A rising edge on TCK in the exit1-IR state or the exit2-IR state with TMS high moves the controller to the update-IR state. The falling edge of that same TCK latches the data in the instruction shift register to the instruction register parallel output. Instructions supported by the MAX16031/MAX16032 and their respective operational binary codes are shown in Table 16.

SAMPLE/PRELOAD: This is a mandatory instruction for the IEEE 1149.1 specification that supports two functions. The digital I/Os of the device are sampled at the boundary scan test data register without interfering with the normal operation of the device by using the capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the boundary scan test data register through TDI using the shift-DR state.

BYPASS: When the BYPASS instruction is latched into the instruction register, TDI connects to TDO through the 1-bit bypass test data register. This allows data to pass from DTDI to TDO without affecting the device's normal operation.

EXTEST: This instruction allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled through the update-IR state, the parallel outputs of all digital outputs are driven. The boundary scan test data register is connected between TDI and TDO. The capture-DR samples all digital inputs into the boundary scan test data register.

IDCODE: When the IDCODE instruction is latched into the parallel instruction register, the identification test data register is selected. The device identification code is loaded into the identification test data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR is used to shift the identification code out serially through TDO. During test-logic-reset, the identification code is forced into the instruction register. The ID code always has a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. See Table 17.

Table 16. JTAG Instruction Set

INSTRUCTION	BINARY CODE	SELECTED REGISTER/ACTION
BYPASS	11111	Bypass
IDCODE	00000	Identification
SAMPLE/PRELOAD	00001	Boundary scan
EXTEST	00010	Boundary scan
USERCODE	00100	User-code data
LOAD ADDRESS	01000	Memory address
READ DATA	01001	Memory read
WRITE DATA	01010	Memory write
REBOOT	01100	Resets the device
SAVE	01101	Stores current fault information in EEPROM

Table 17. 32-Bit Identification Code

MSB			LSB
Version (4 bits)	Device ID (16 bits)	Manufacturer ID (11 bits)	Fixed value (1 bit)
0000	0000000000000001	00011001011	1

Table 18. 32-Bit User-Code Data

MSB		
D.C. (don't cares)	I²C/SMBus Slave Address	User identification (firmware version)
00000000000000000	See Table 15	r5Eh[7:0] contents

USERCODE: When the USERCODE instruction is latched into the parallel instruction register, the user-code data register is selected. The device user code is loaded into the user-code data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR is used to shift the user code out serially through TDO. See Table 18.

LOAD ADDRESS: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16031/MAX16032. When the LOAD ADDRESS instruction is latched into the instruction register, TDI connects to TDO through the 8-bit memory address test data register during the shift-DR state.

READ: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16031/MAX16032. When the READ instruction is latched into the instruction register, TDI connects to TDO through the 8-bit memory read test data register during the shift-DR state.

WRITE: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16031/MAX16032. When the WRITE instruction is latched into the instruction register, TDI connects to TDO through the 8-bit memory write test data register during the shift-DR state.

REBOOT: This is an extension to the standard IEEE 1149.1 instruction set to initiate a software-controlled reset to the MAX16031/MAX16032. When the REBOOT instruction is latched into the instruction register, the MAX16031/MAX16032 reset and immediately begin their boot-up sequence.

SAVE: This is an extension to the standard IEEE 1149.1 instruction set that triggers a fault log. When the SAVE instruction is latched into the instruction register, the MAX16031/MAX16032 copy fault information from registers to EEPROM.

Boundary Scan

The boundary scan feature allows access to all the digital I/O connections of the MAX16031/MAX16032. If the sample/preload or the EXTEST instruction is loaded into the instruction register, TDI connects to TDO through the 198-bit boundary scan register. Each digital I/O pin corresponds to 1 bit (or 2 bits, in the case of the A0 and A1 pins) of the boundary scan register. The rest of the boundary scan bits are reserved and are loaded with zeros.

When the sample/preload instruction is executed, the current state of the digital outputs is latched into the boundary scan register and is shifted out through TDO. This instruction may be executed without interrupting normal operation of the part. When the EXTEST instruction is executed, the boundary scan register bits supersede the normal functionality of the I/O pins: an output mirrors the state of the corresponding boundary scan register bit.

Table 19 lists the function of each boundary scan register bit. Since the I²C address select pins have three possible states, 2 boundary scan register bits are required to represent them. These bits are defined in Table 20.

Applications Information

Layout and Bypassing

Bypass V_{CC}, DBP, and ABP each with a 1µF capacitor to GND. Bypass RBP with a 2.2µF capacitor to GND. Avoid routing digital return currents through a sensitive analog area, such as an analog supply input return path or ABP's bypass capacitor ground connection. Use dedicated analog and digital ground planes.

Table 19. Boundary Cell Order

BOUNDARY CELL NO.	DESCRIPTION/PIN
0–147	Reserved
148	GPIO1 (output)
149	GPIO2 (output)
150	SDA (output)
151	$\overline{\text{ALERT}}$
152	$\overline{\text{FAULT2}}$
153	$\overline{\text{FAULT1}}$
154	$\overline{\text{OVERT}}$
155	$\overline{\text{RESET}}$
156	$\overline{\text{OVERC}}$
157–182	Reserved
183	GPIO2 (input)
184	GPIO1 (input)
185	SDA (input)
186	A0b
187	A0a
188	A1b
189	A1a
190	SCL
191–197	Reserved

Table 20. Address Pin State Decode

A0A A0B	A0 PIN STATE
0 0	High impedance
0 1	Low
1 0	High
1 1	Not defined

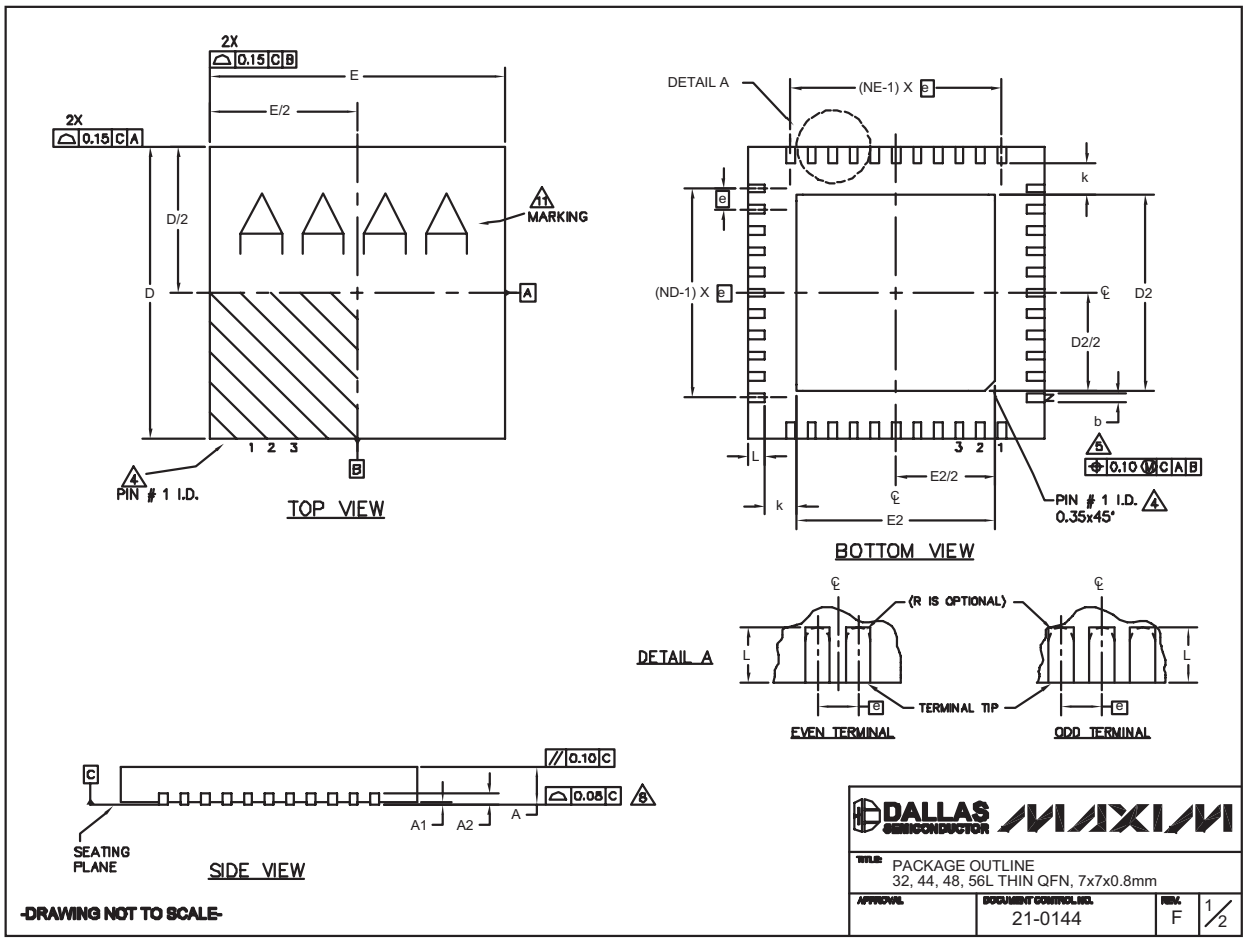
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



EEPROM-Based System Monitors with Nonvolatile Fault Memory

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS							
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877-4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–
T4877-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877M-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-2	–	5.40	5.50	5.60	5.40	5.50	5.60	–

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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Revision History

Pages changed at Rev 1: 1, 41, 42